

PCB STACK UP

6L Dis.

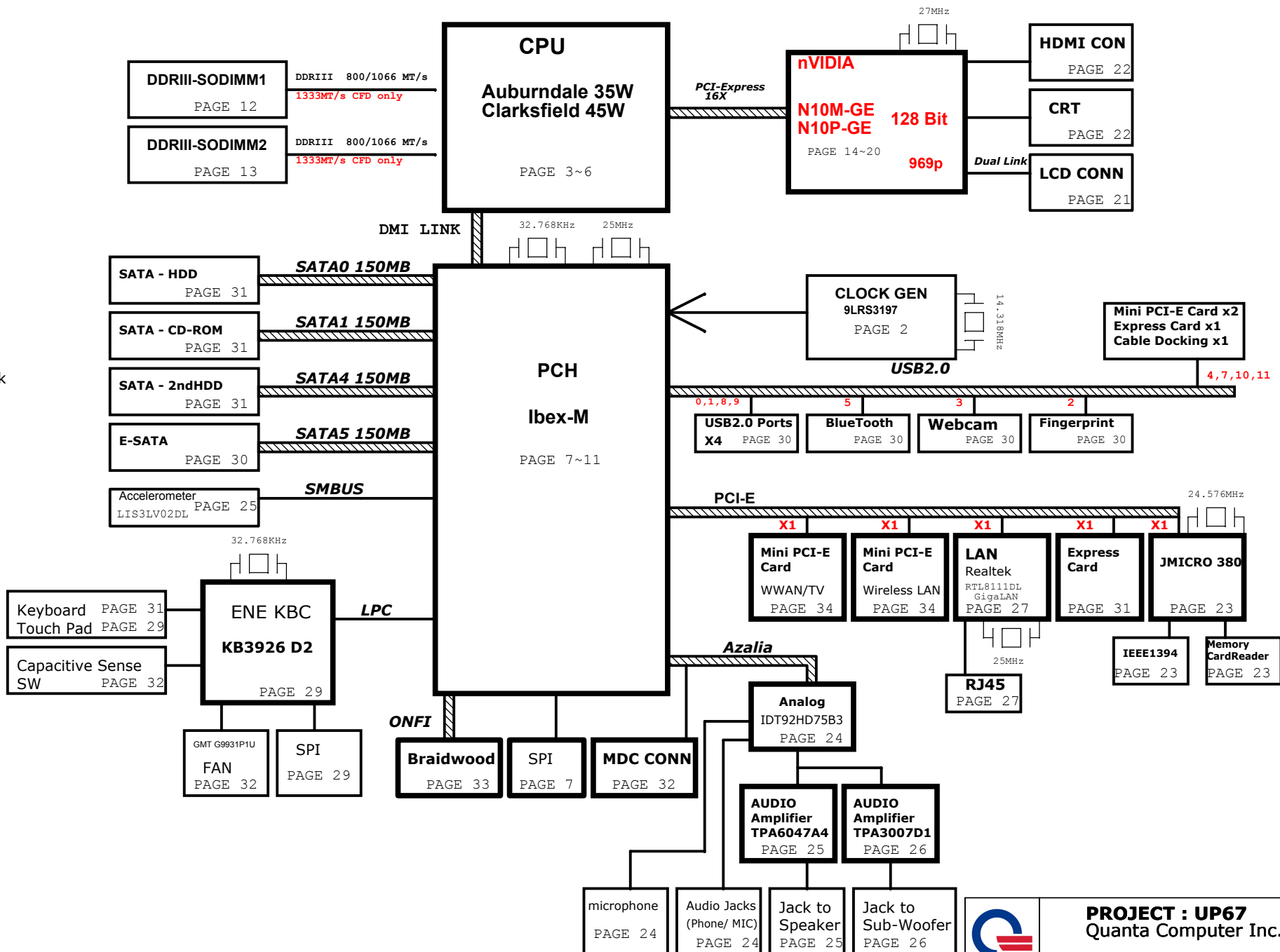
Jones/Cujo 2.0 (UP6/7) BLOCK DIAGRAM

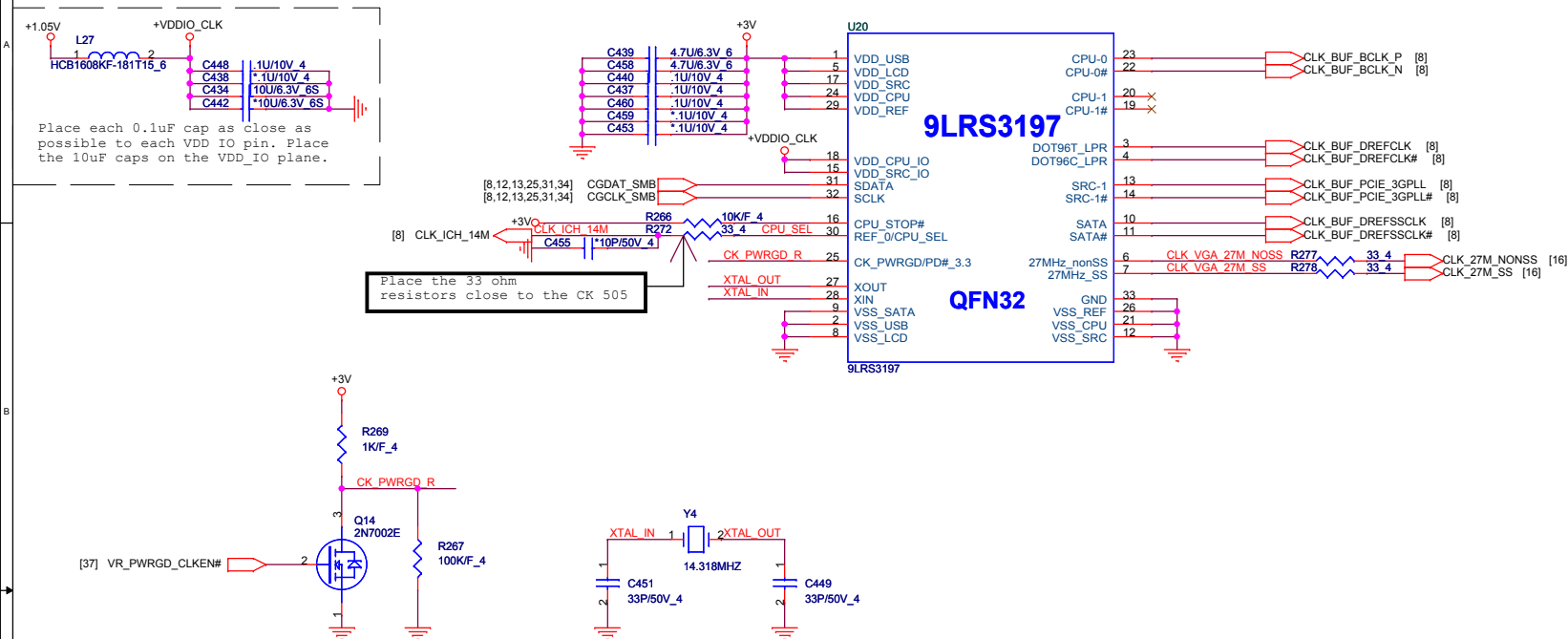
01

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : BOT

- Cable Docking**
- VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PAGE 32

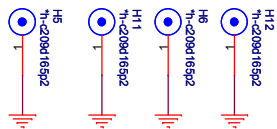
- SYSTEM POWER RT8206B PAGE 35
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 36
- CPU CORE ISL6251A PAGE 41
- VGACORE(1.025V) RT8208A PAGE 38
- DDR III SMDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 39
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 40



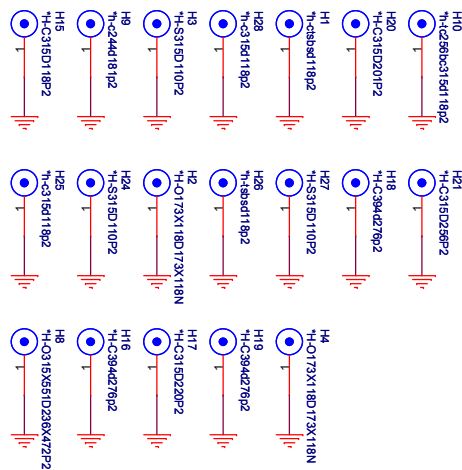


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

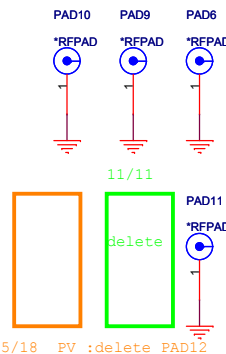
CPU bracket Hole.



M/B Screw Hole



RF PAD



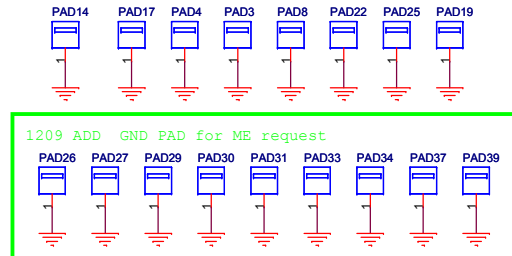
ME PAD



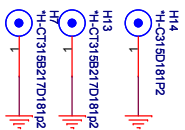
Routed spring



ME-Ground Pad

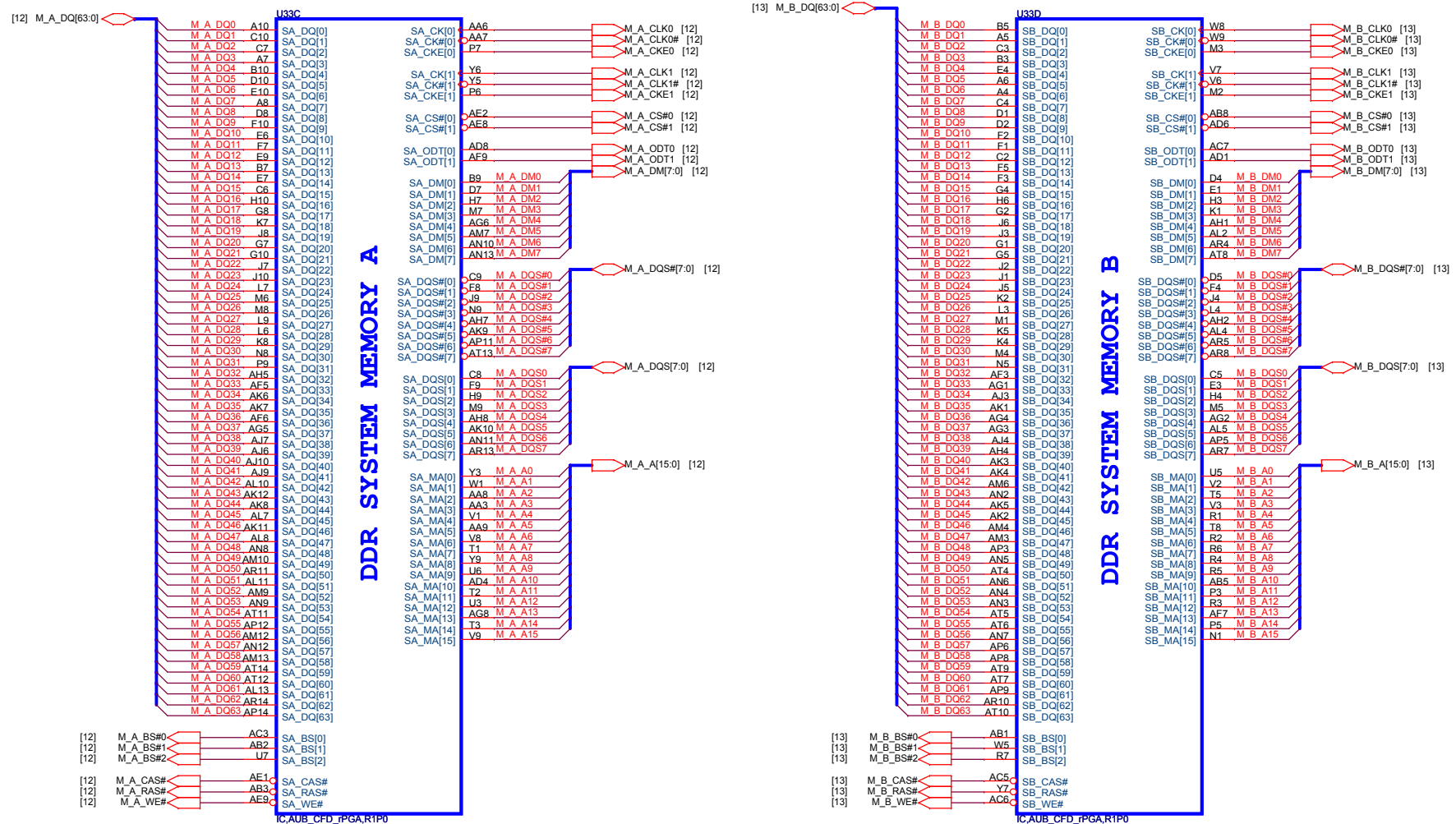


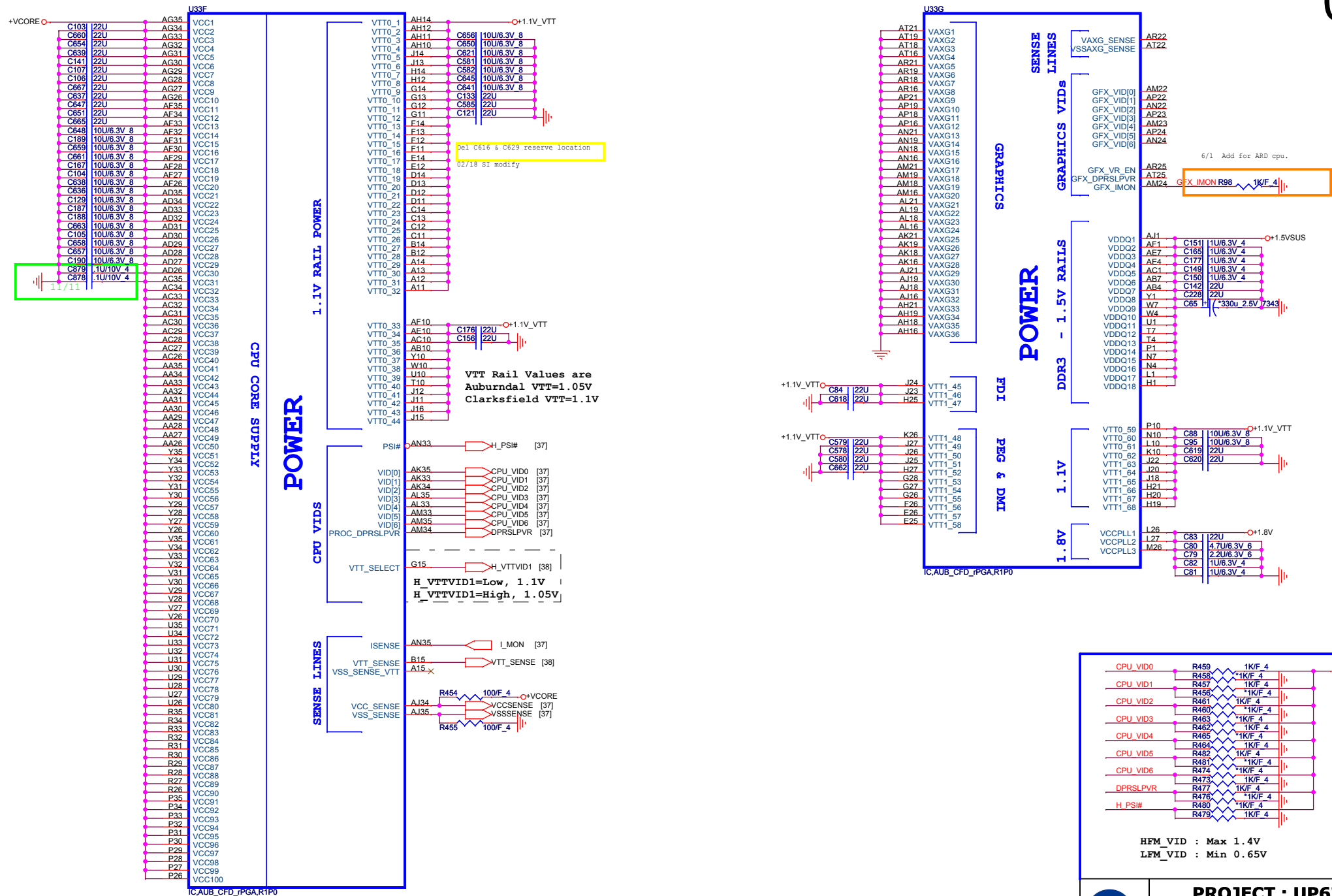
VGA bracket Hole.



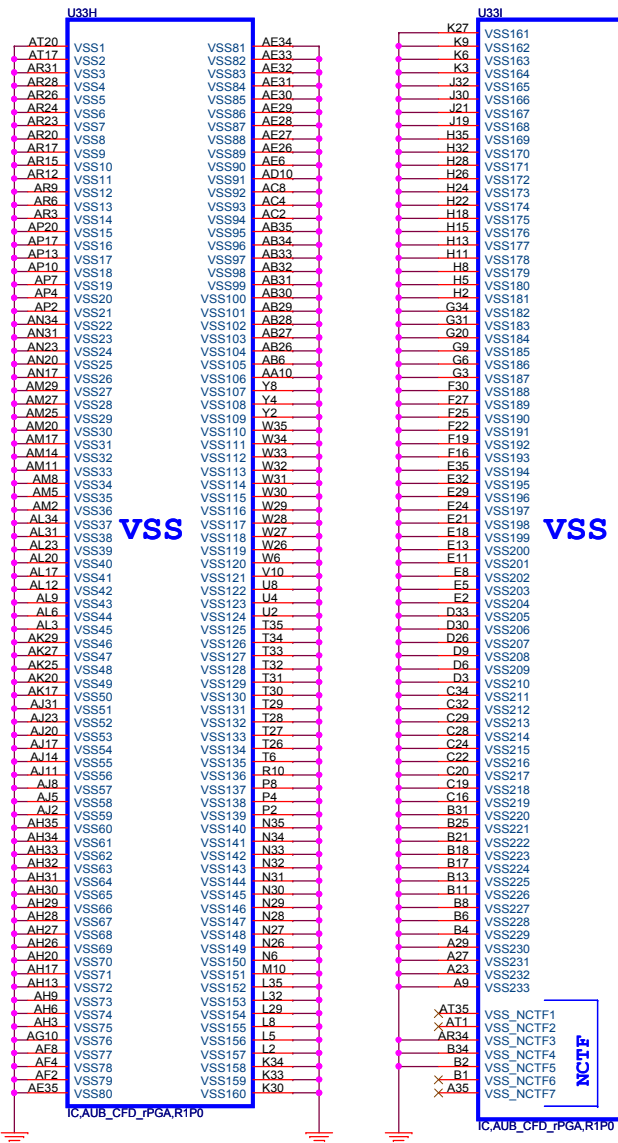
U33A

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



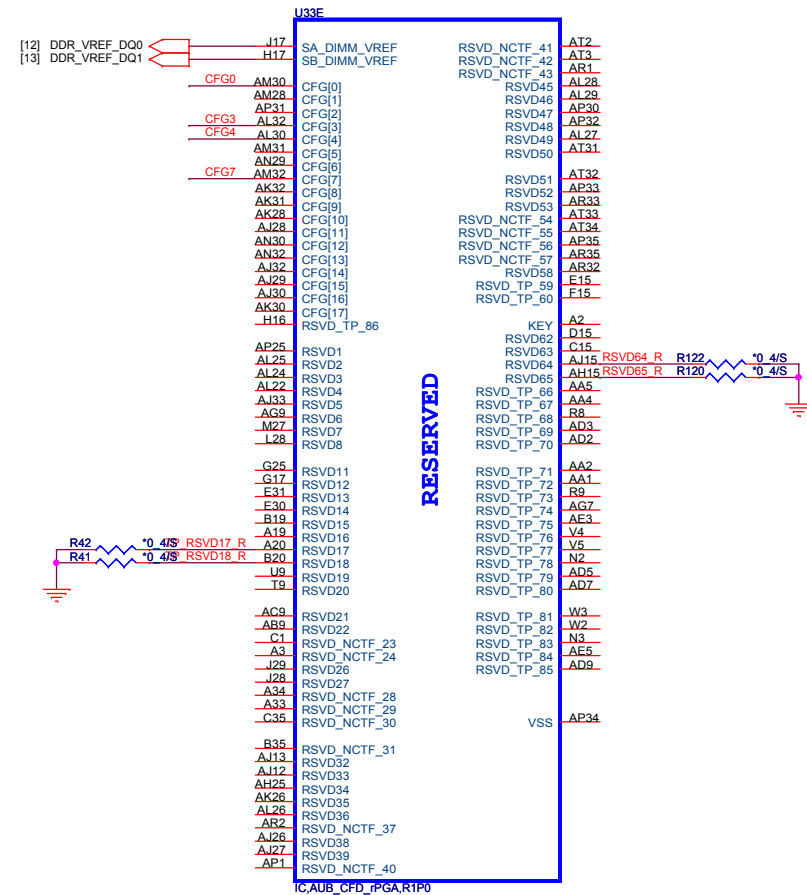


AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01k Ω \pm 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



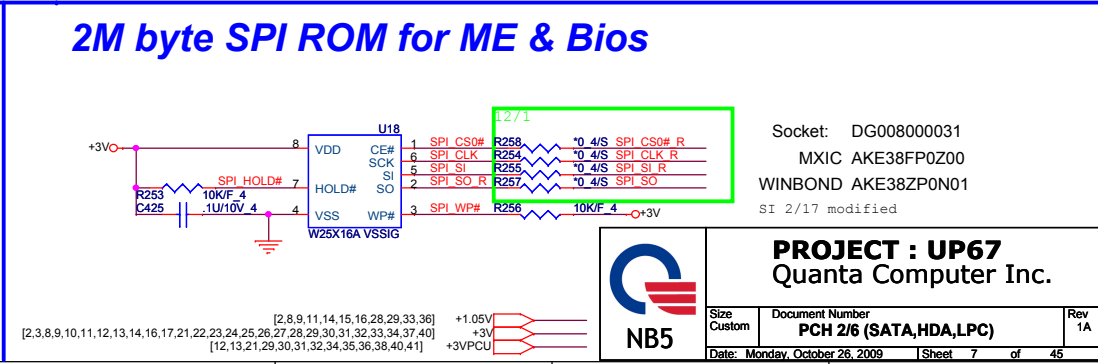
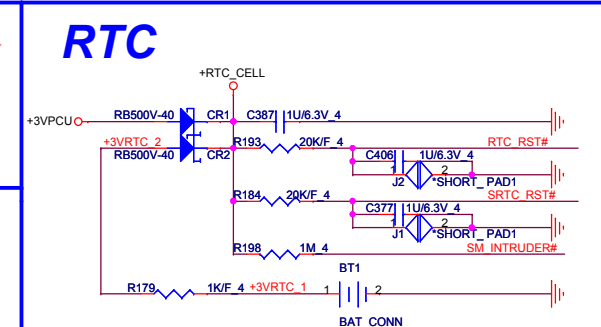
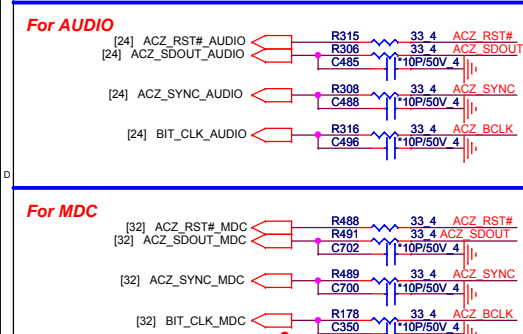
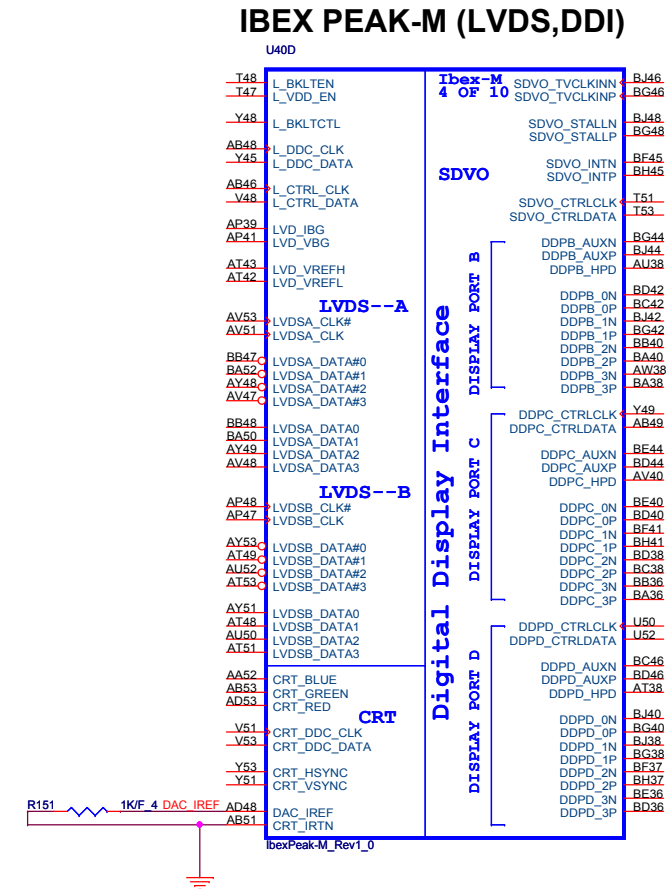
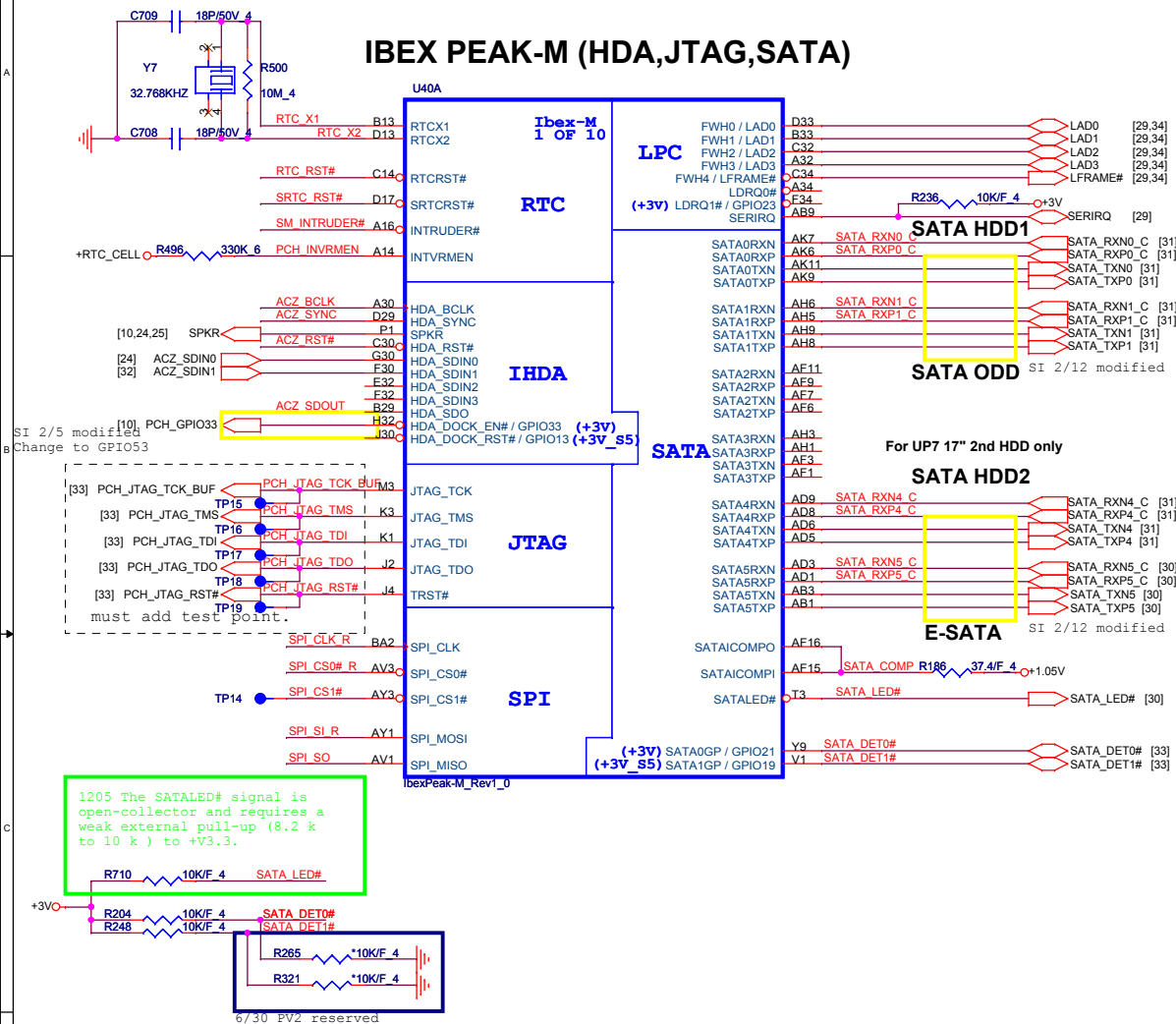
```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```



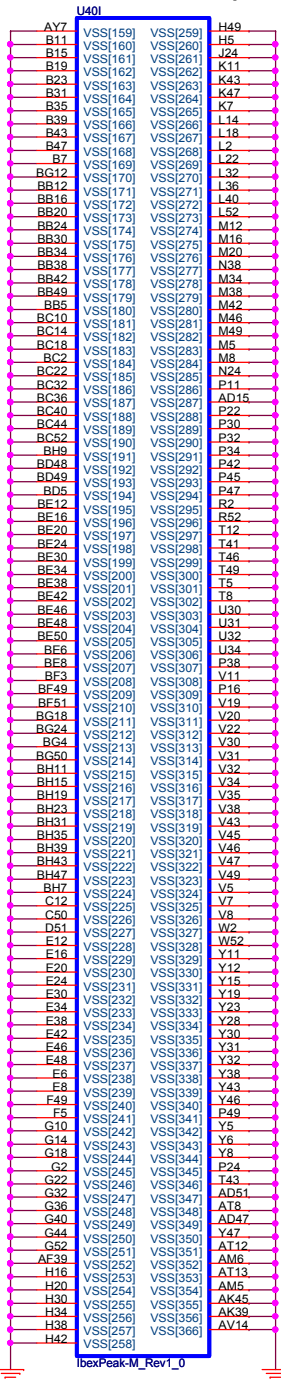
PROJECT : UP67
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Size Custom	Document Number PROCESSER 4/4(GND)	Rev 1A
Date: Monday, October 26, 2009		Sheet 6 of 45

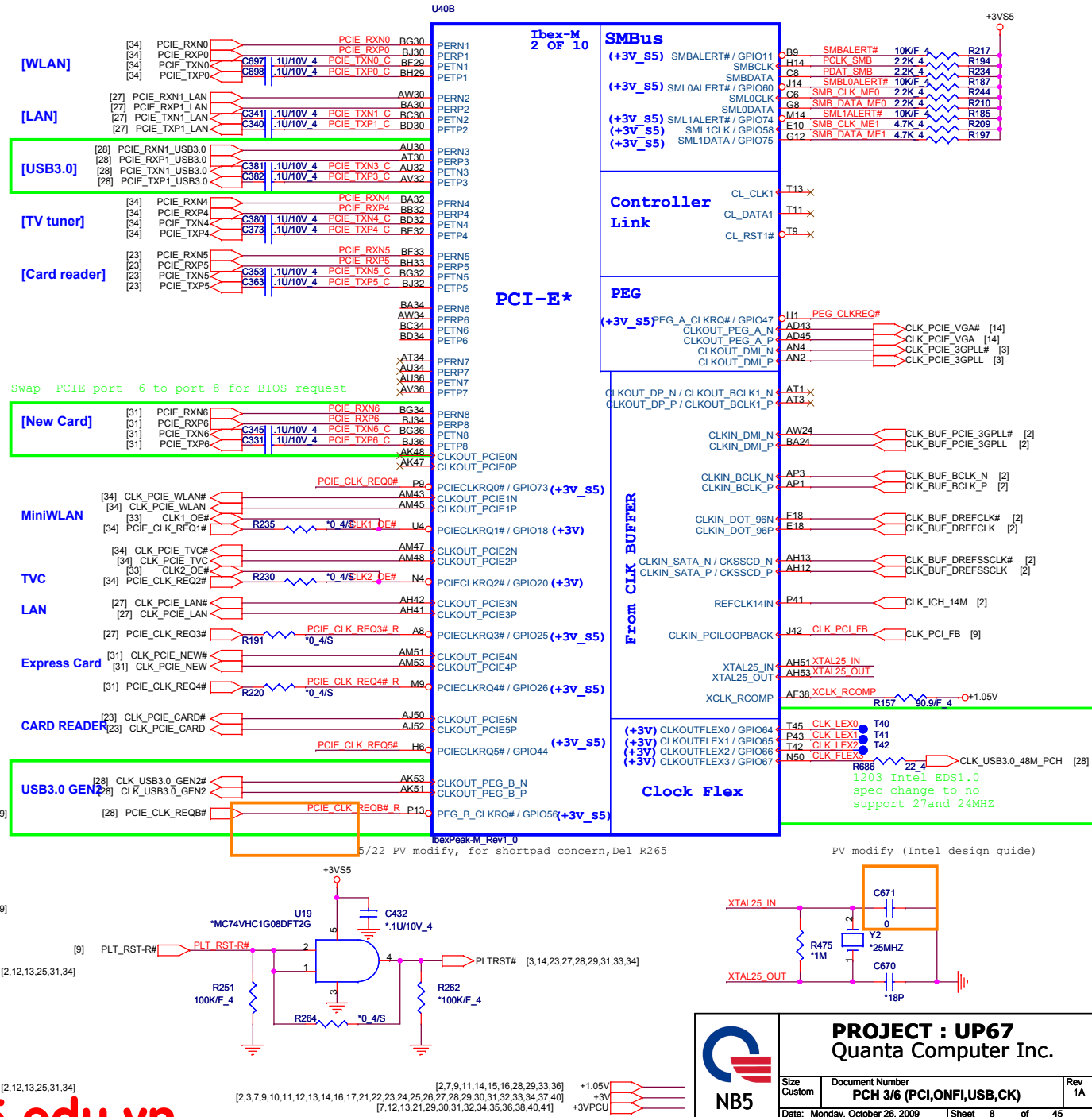
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs



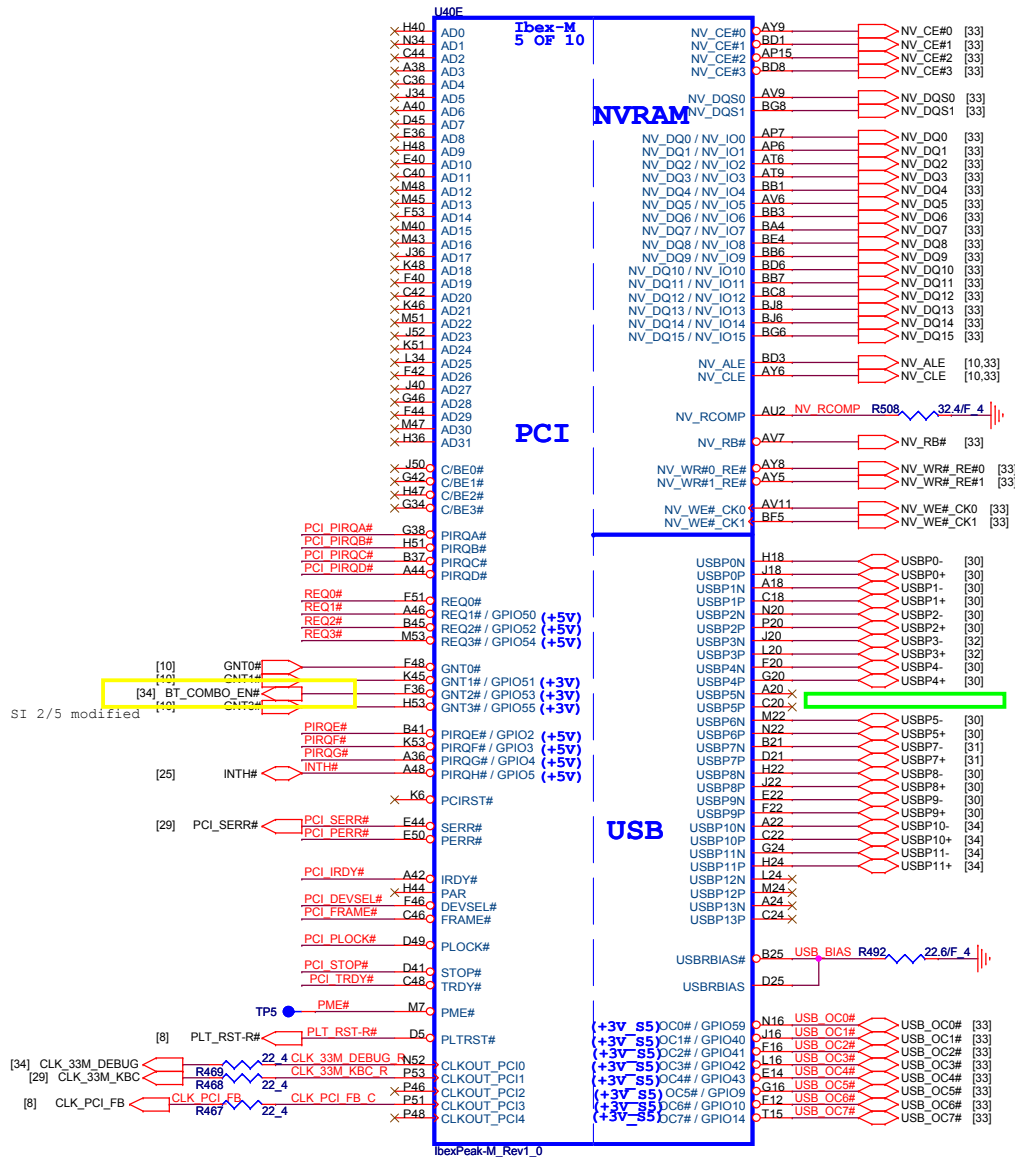
IBEX PEAK-M (GND)



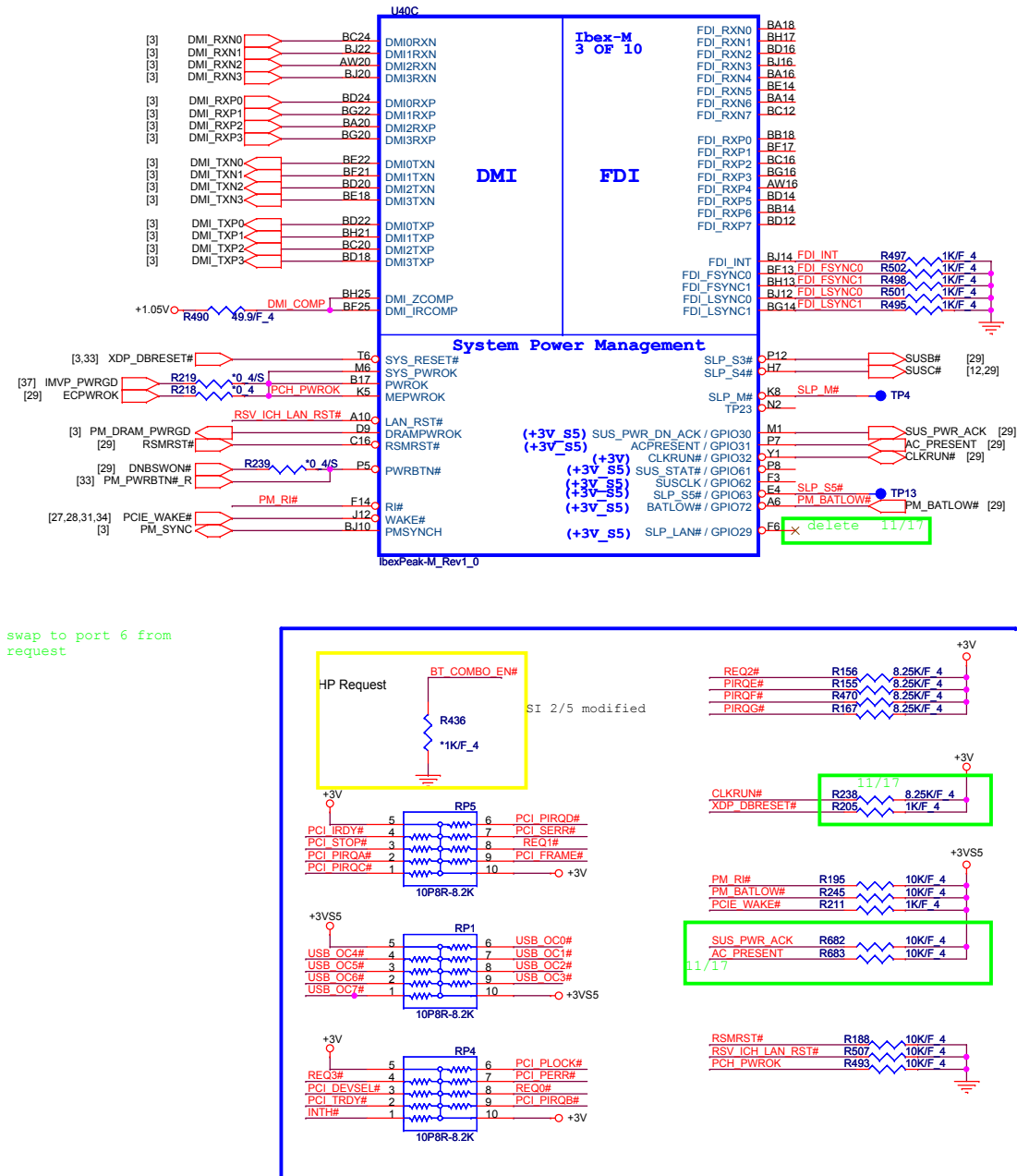
IBEX PEAK-M (PCI-E,SMBUS,CLK)



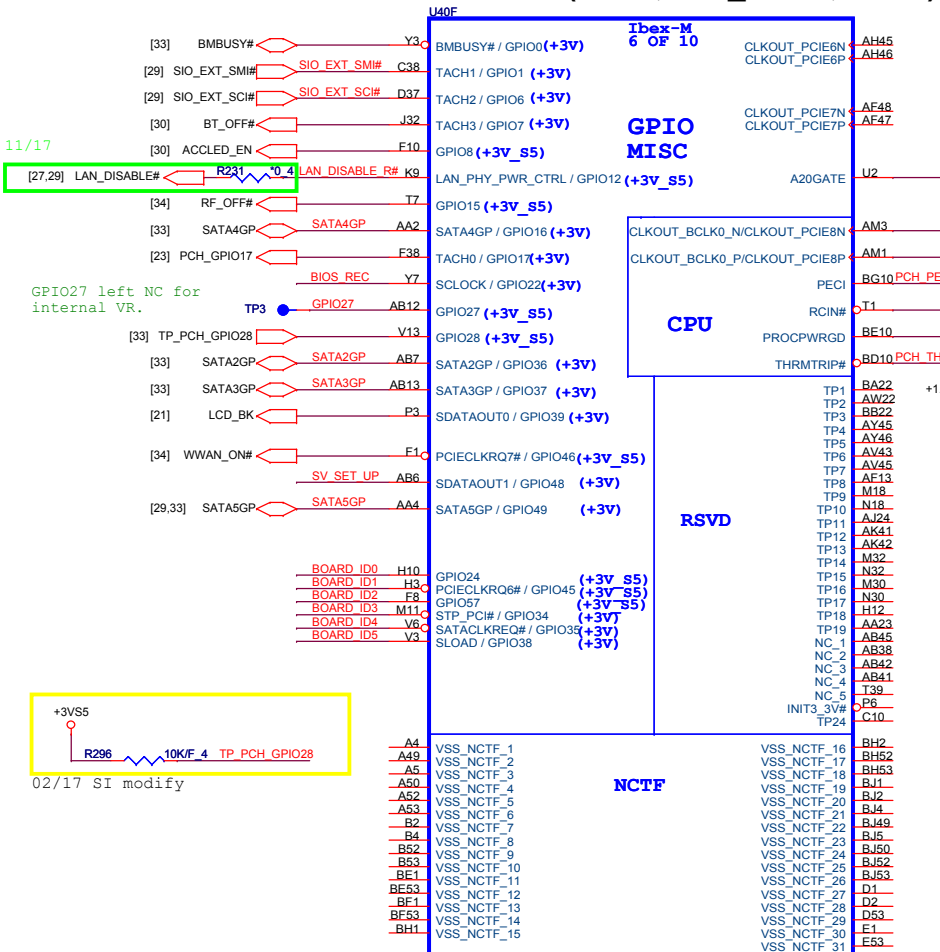
IBEX PEAK-M (PCI,USB,NVRAM)



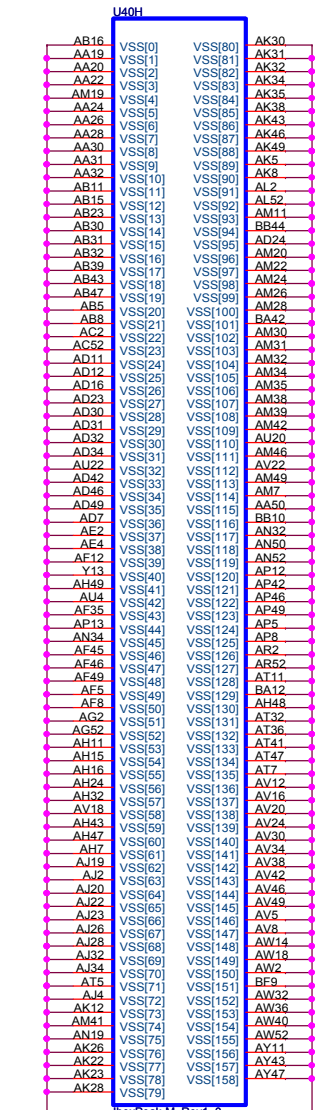
IBEX PEAK-M (DMI,FDI,GPIO)



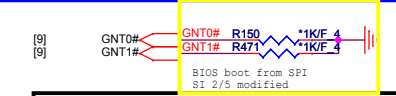
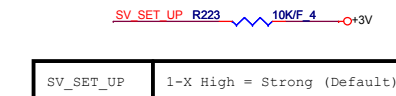
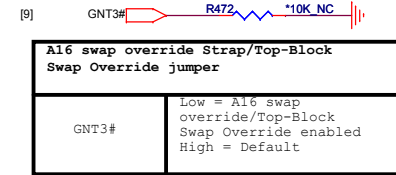
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



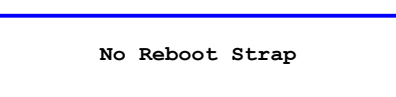
10



PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



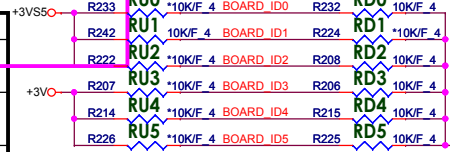
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

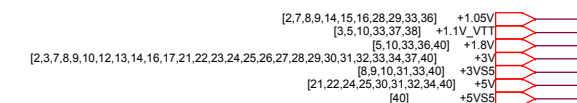
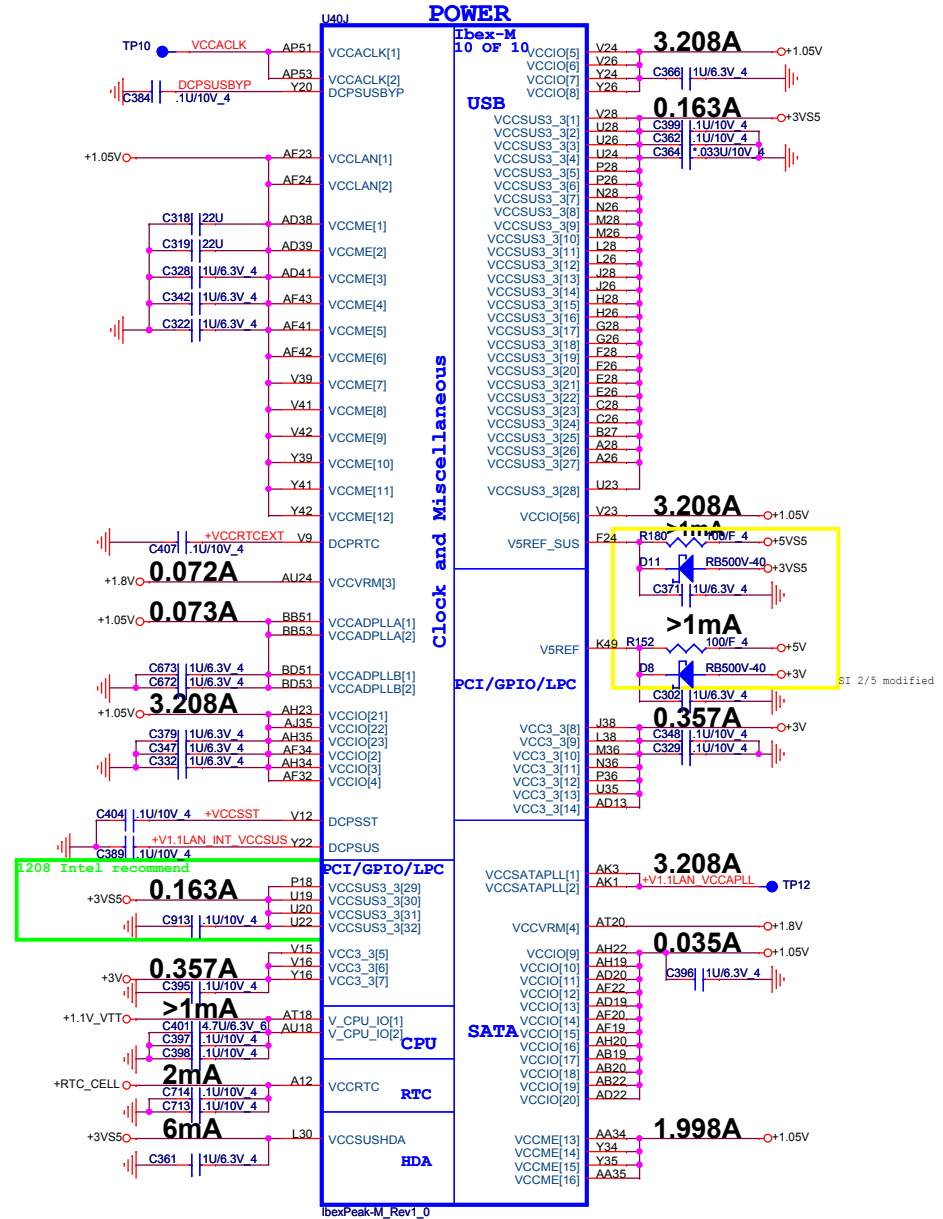
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UP6/7	0=UP6 1=UP7					
UMA/Dis.		0=UMA 1=Dis.				
Project name			0=Jones/Cujo 2.0 (Clarkfield) 1=Jones/Cujo 2.1 (Auburndale UMA)			
ROM Size				0= 2M 1= 4M		

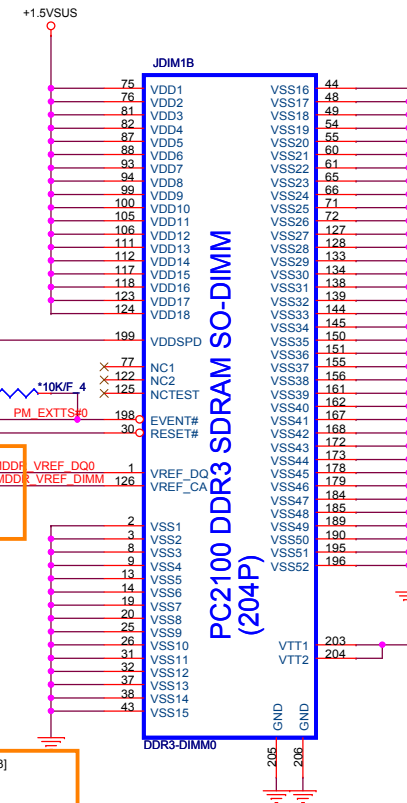
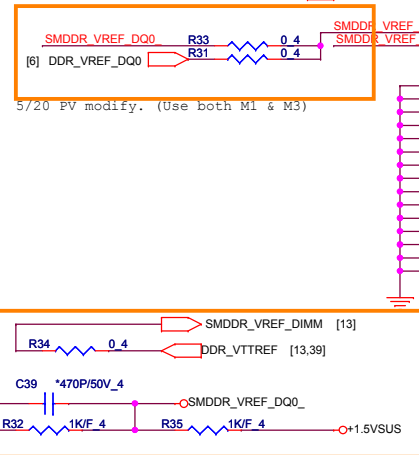
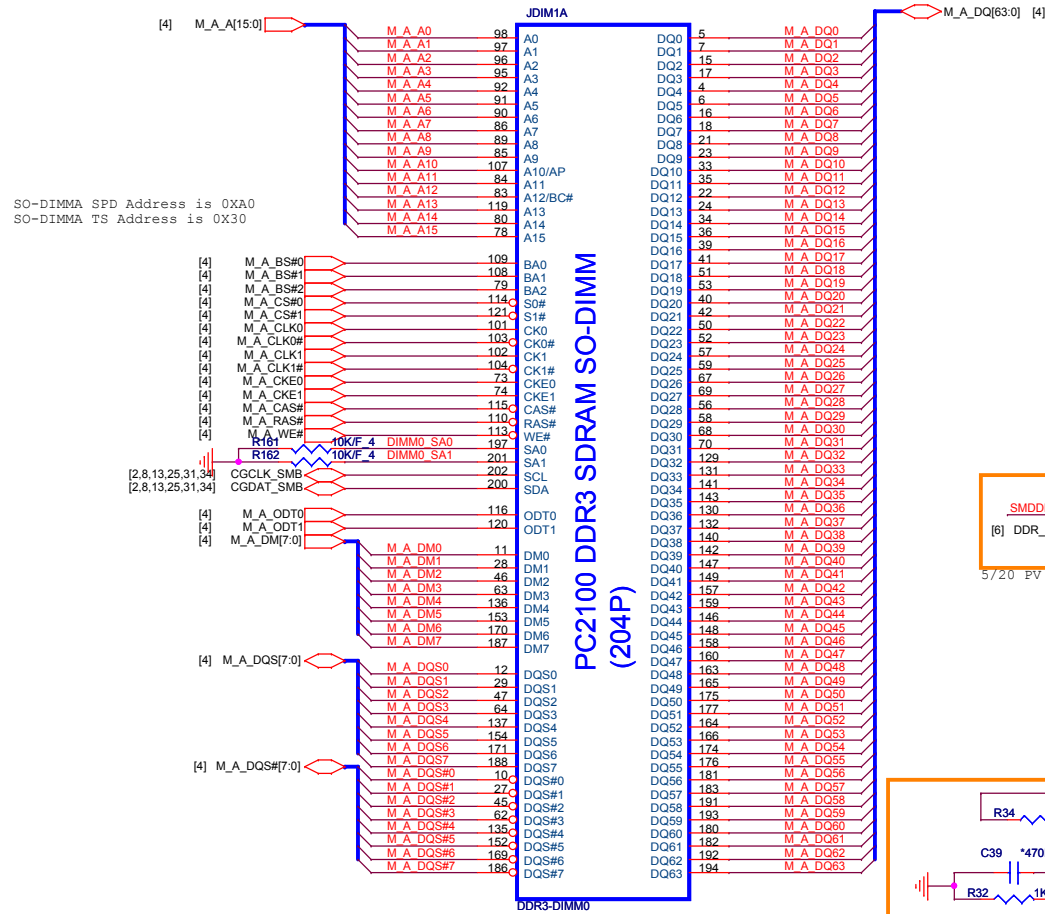


<http://sualaptop365.edu.vn>

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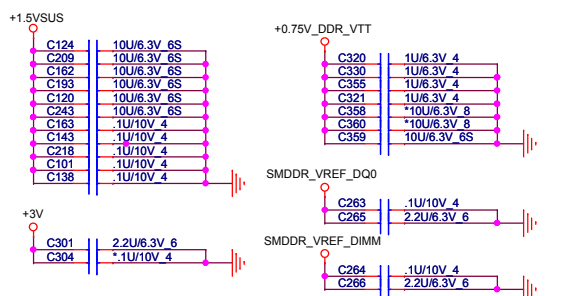
Size Custom	Document Number	Rev 1A
	PCH 4/6 (GPIO & Strap)	
Date: Monday, October 26, 2009	Sheet 10 of 45	





Place these Caps near So-Dimm0.

5/20: NA for INT recomment



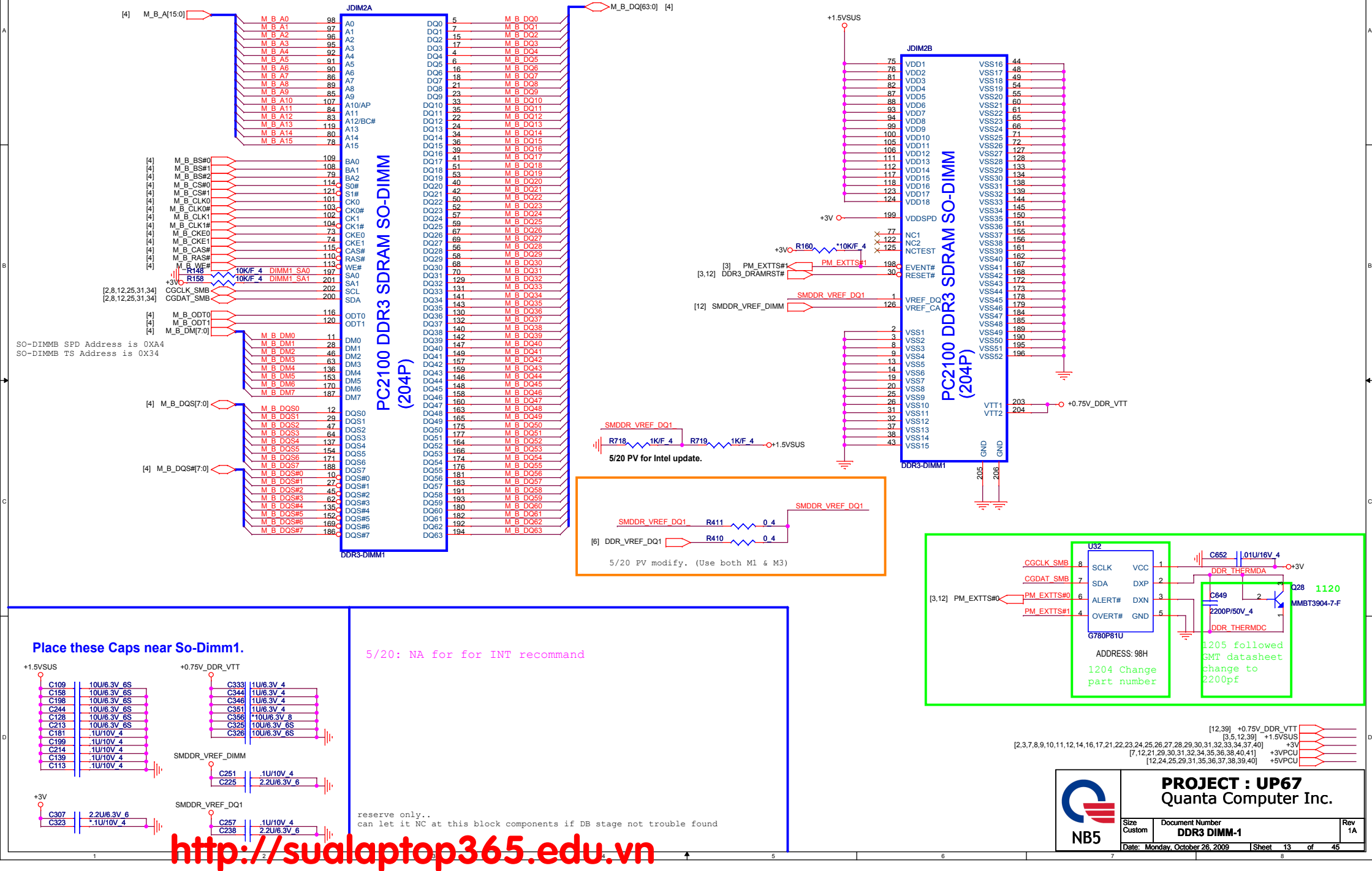
reserve only...
can let it NC at this block components if DB stage not trouble found

[13,39] +0.75V_DDR_VTT
[3,5,13,39] +1.5VSUS
[2,3,7,8,9,10,11,13,14,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,40] +3V
[7,13,21,29,30,31,32,34,35,36,38,40,41] +3VPCU
[24,25,29,31,35,36,37,38,39,40] +5VPCU

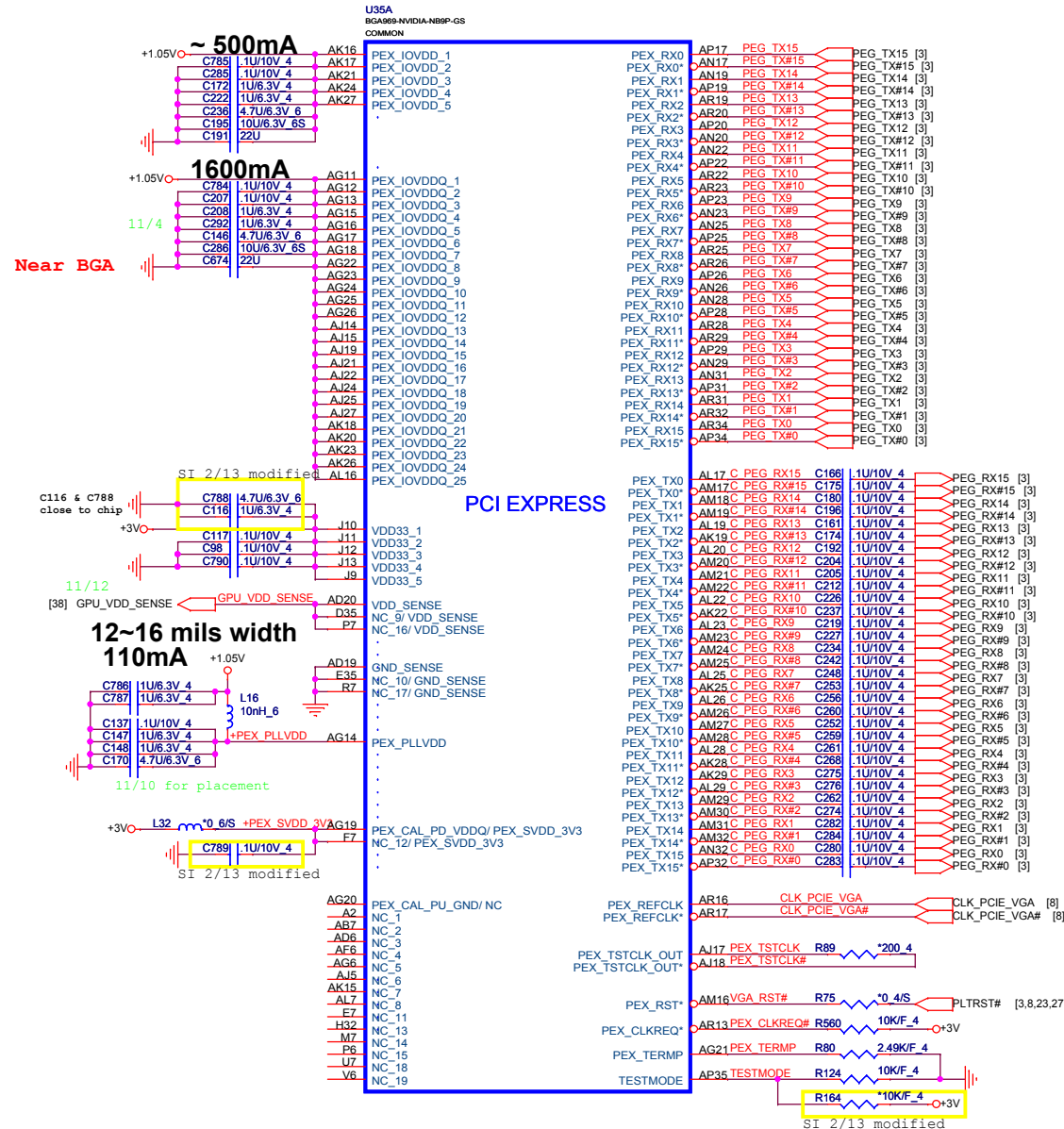


PROJECT : UP67
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Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
Date: Monday, October 26, 2009	Sheet 12 of 45	



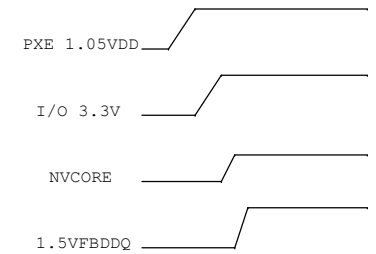
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD > 2.2A



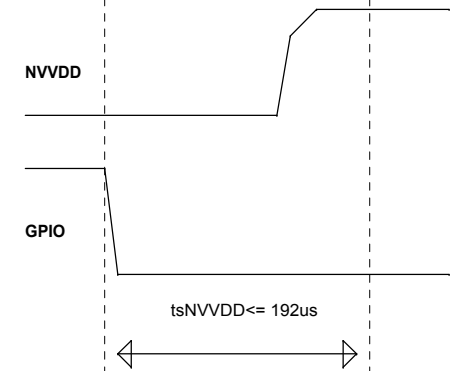
VGA Thermal Circuit

0514: PV modify
Delete Reserved thermal circuit

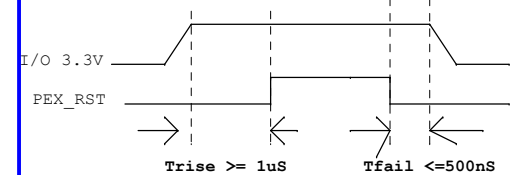
power up sequence



NB9M: VGACORE +0.90V (Normal) , +1.09V
NVVDD Maximum Settling Time



PEX_RST timing



[2,3,7,8,9,10,11,12,13,16,17,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40] [2,7,8,9,11,15,16,28,29,33,36] +1.05V
+3V

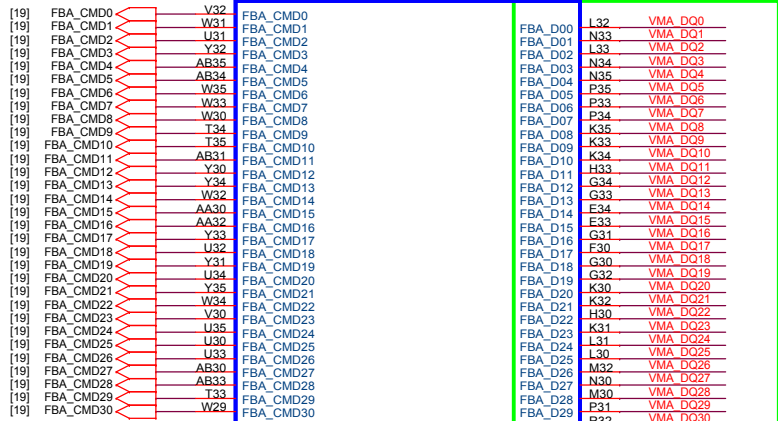


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Quanta Computer Inc.

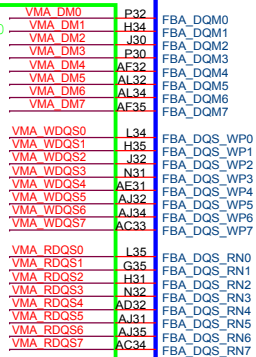
Size Custom Document Number N10X (PCIE I/F) 1/5 Rev 1A
Date: Monday, October 26, 2009 Sheet 14 of 45

U35B
BGA699-NVIDIA-NBSP-GS
COMMON

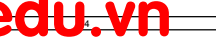
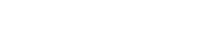
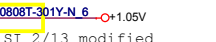
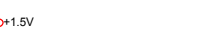
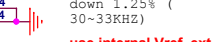
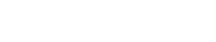
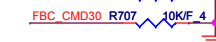
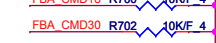
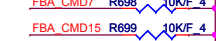
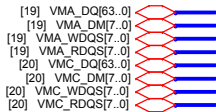
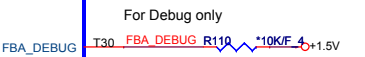
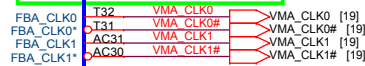
12/02 modify
package for N10



12/02 modify
package for N10

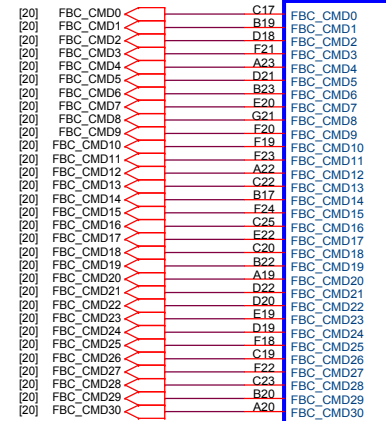


MEMORY I/F A

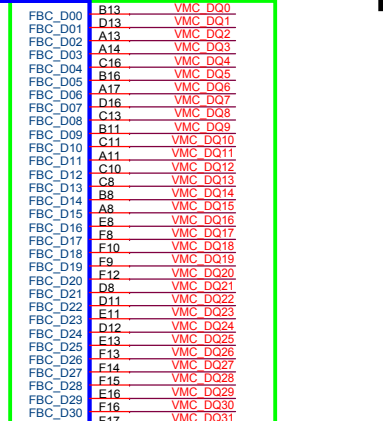
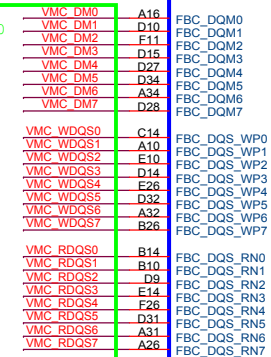


U35C
BGA699-NVIDIA-NBSP-GS
COMMON

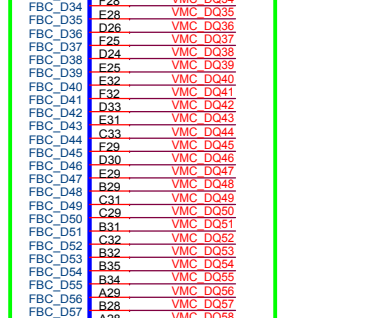
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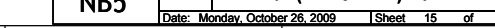
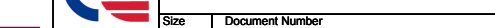
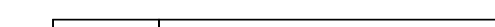
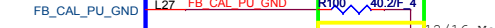
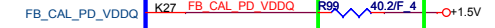
12/02 modify
package for N10



12/02 modify
package for N10



MEMORY I/F C



PROJECT : UP67
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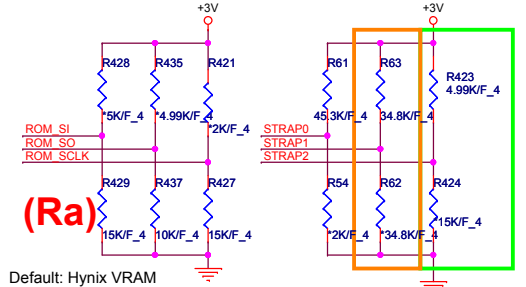
Size	Document Number	Rev
Custom	N10X (MEMORY I/F) 2/5	1A
Date: Monday, October 26, 2009	Sheet 15 of 45	

CHIP	PCI_DEVID:	STRAP2
N10P-GE	0x0A28	1000 PU 5K
N10M-GE	0x0A68	1000 PU 5K

SEE Datasheet for details on N10P Straps!

PCI_DEVID[4]/SUBVENDOR 1211 DEVICE ID CHANGE

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



Default: Hynix VRAM

CS31002FB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502FB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002FB02 (RES CHIP 20K 1/16W +-1% (0402))

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved		
0101	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
0110	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	
XXXX				
XXXX				

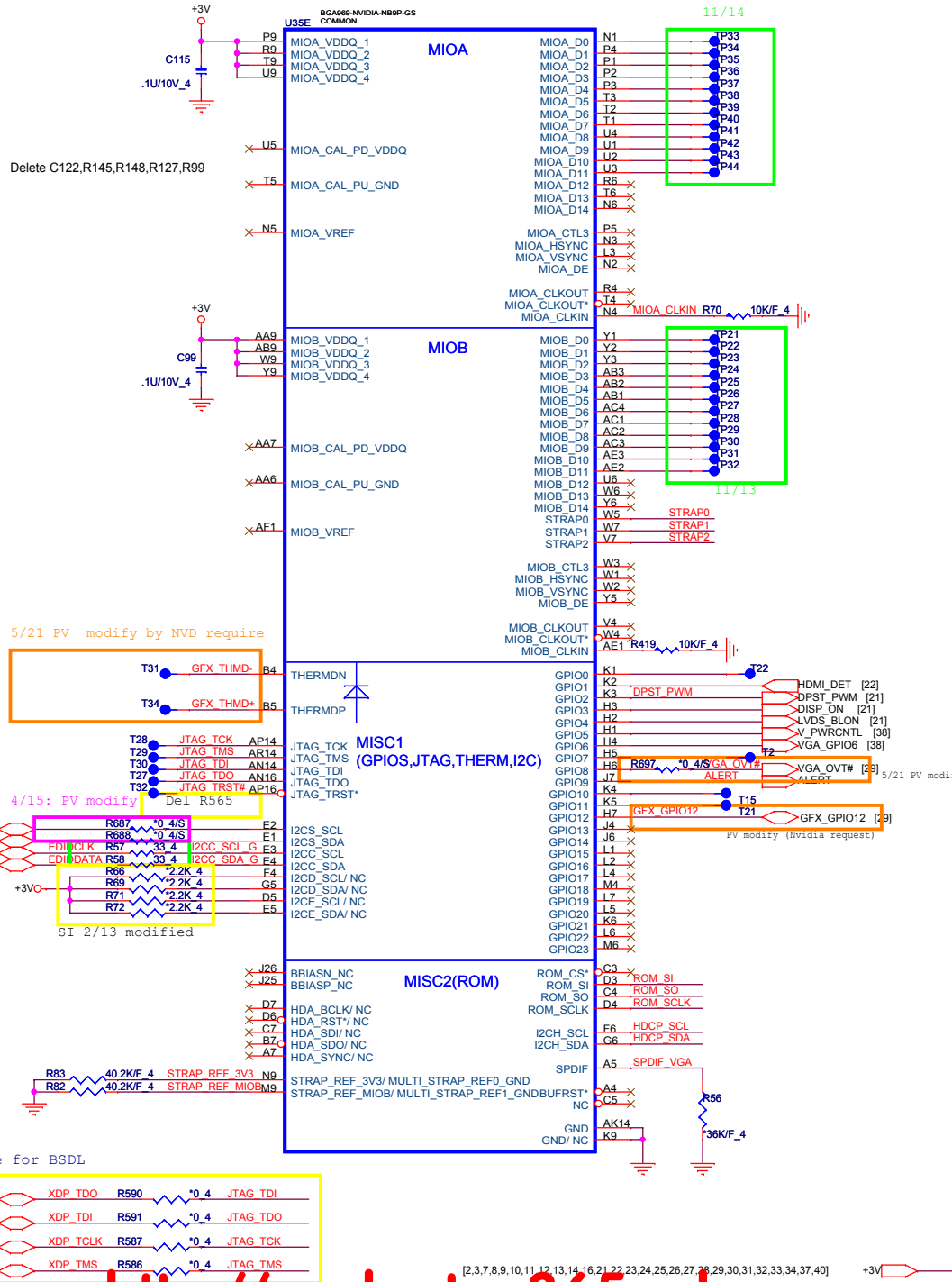
GPIO ASSIGNMENTS

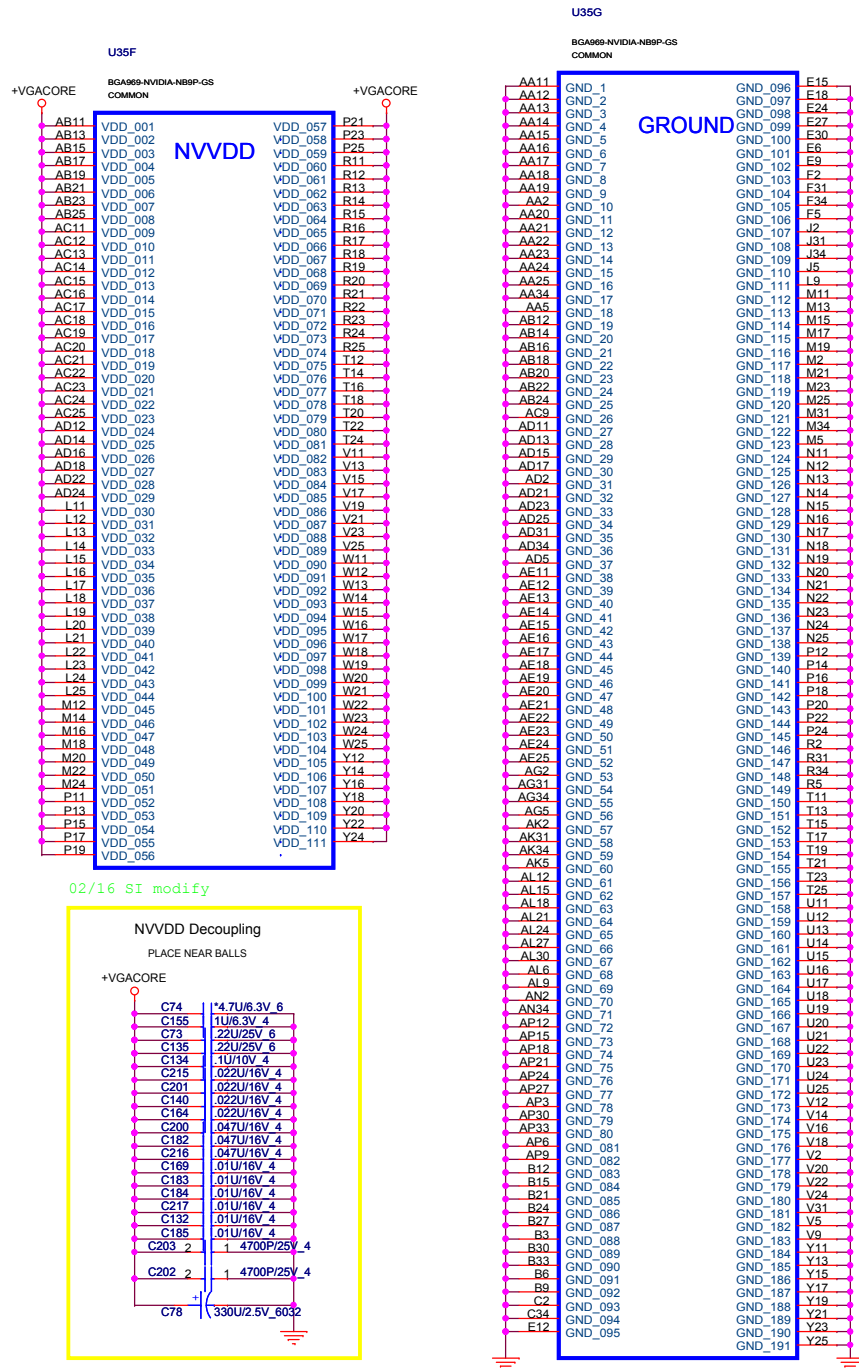
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL



PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number	Rev
	N10X (GPIO & STRAPS) 4/5	2A
Date: Monday, October 26, 2009	Sheet 17 of 45	





Del all VRAM termination
(RP16~RP75)

SI 2/5 modified



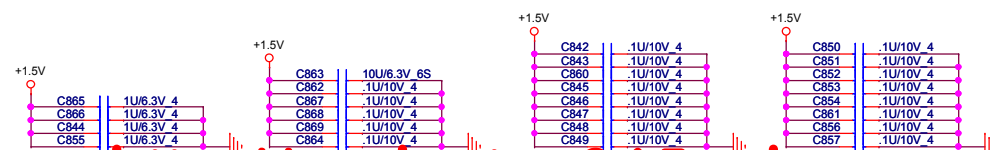
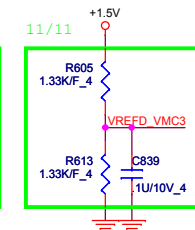
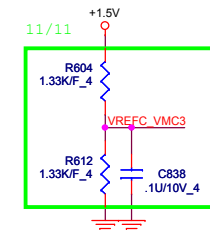
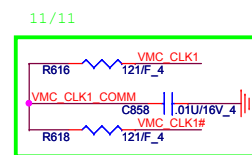
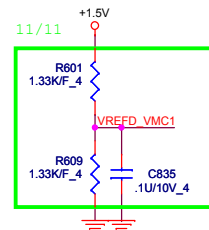
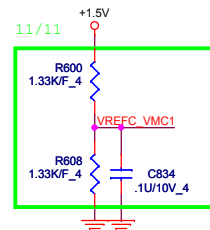
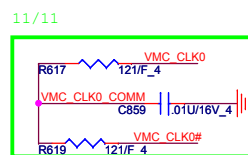
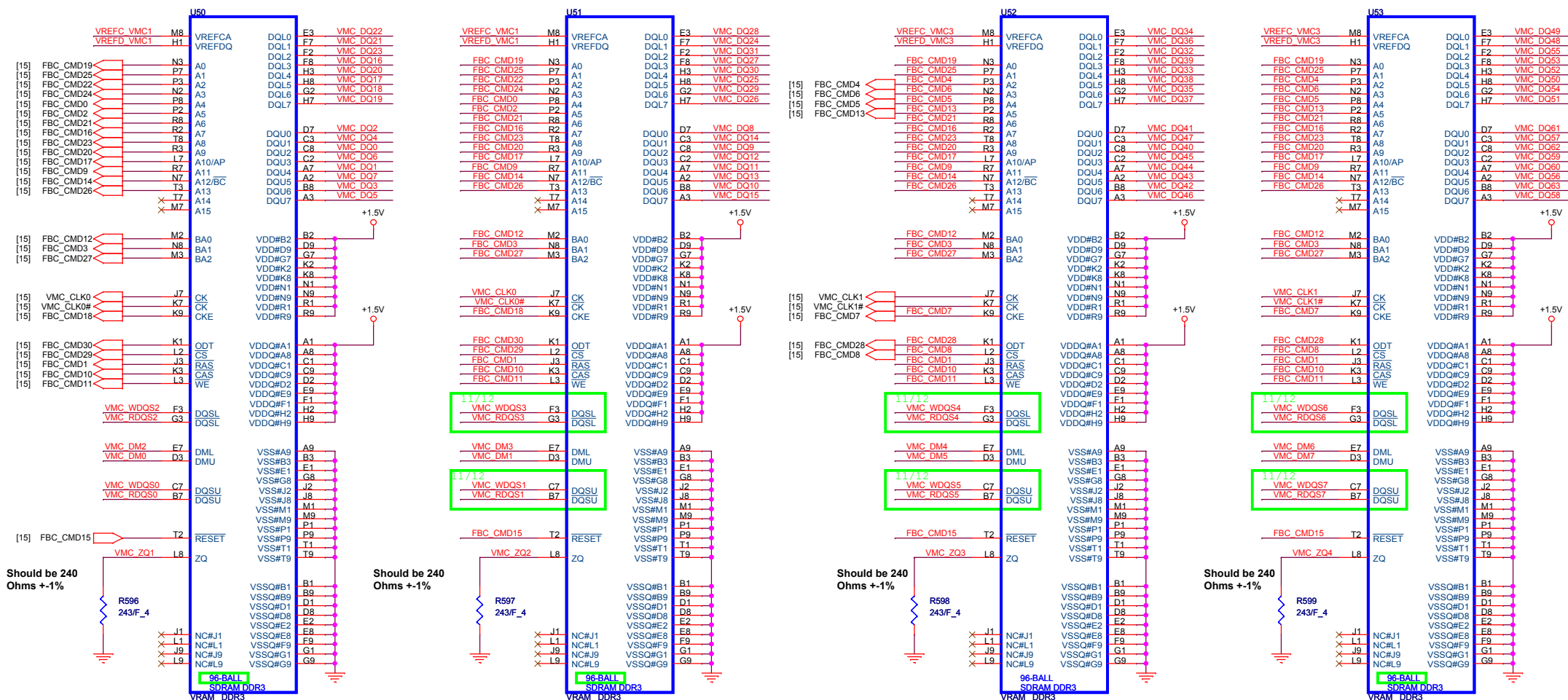
PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number N10X (POWER & GND) 5/5	Rev 2A
Date: Monday, October 26, 2009 Sheet 18 of 45		

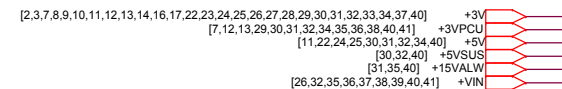
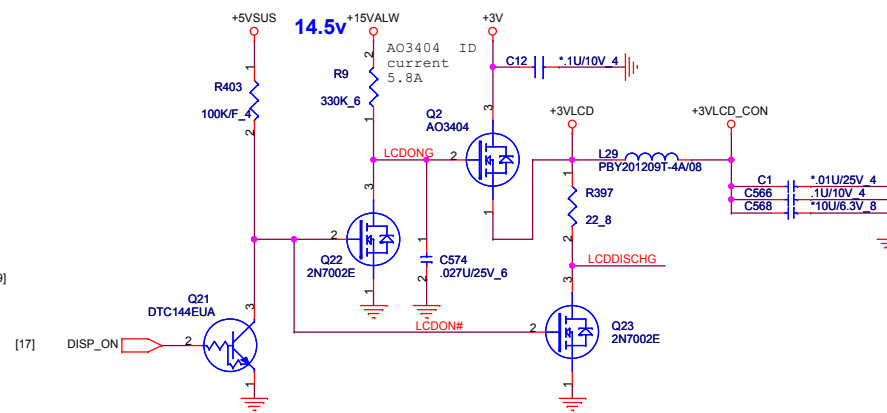
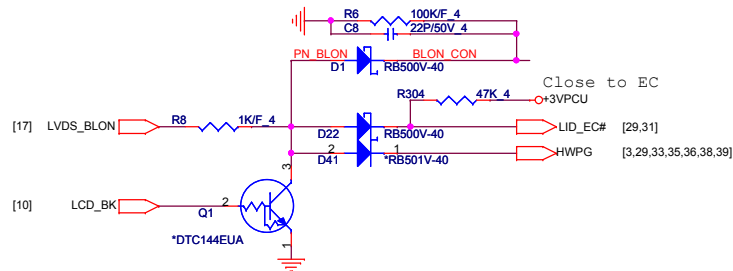
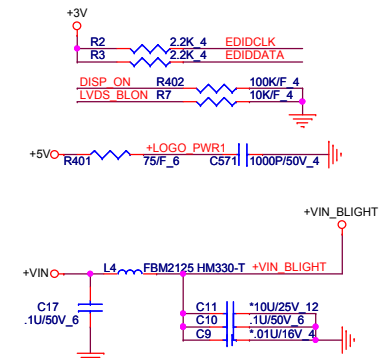
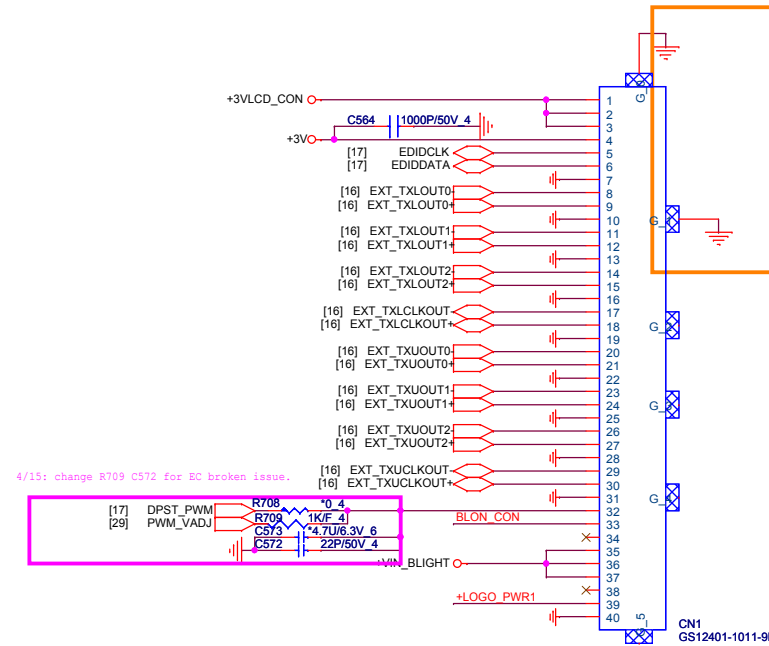


CHANNEL B: 256MB/512MB DDR3

```
[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]
```



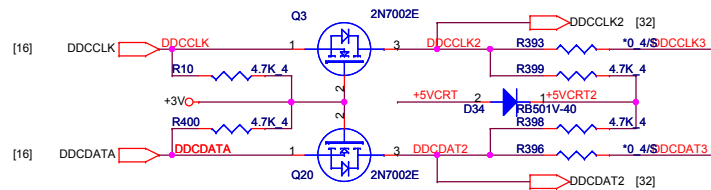
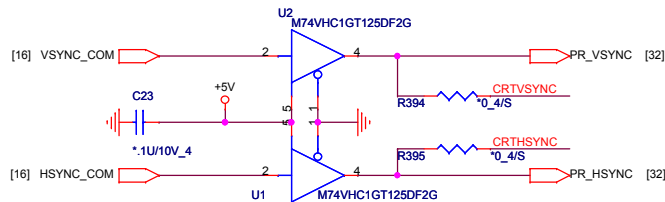
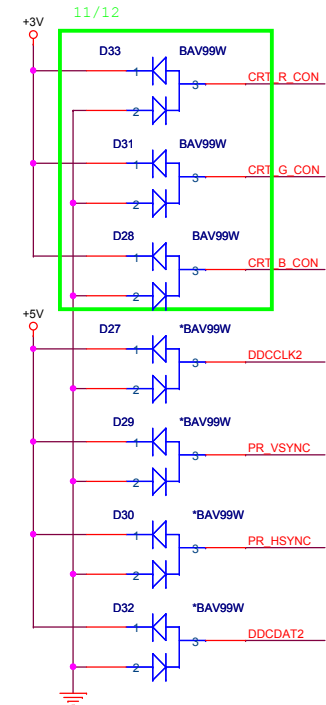
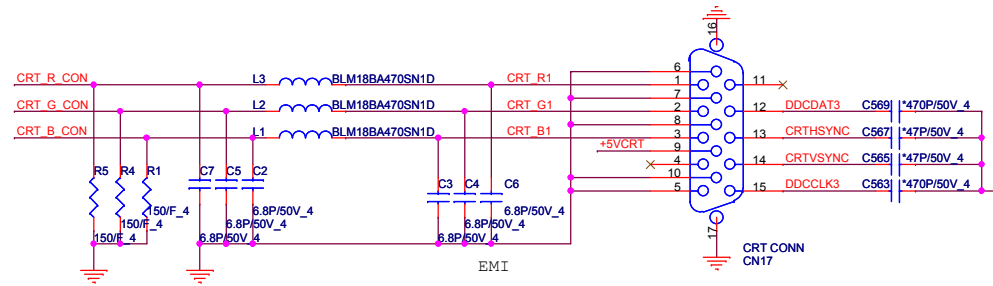
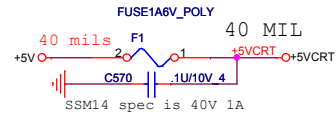
5/20: change PIN 41,PIN42 to GND pad for EMI.



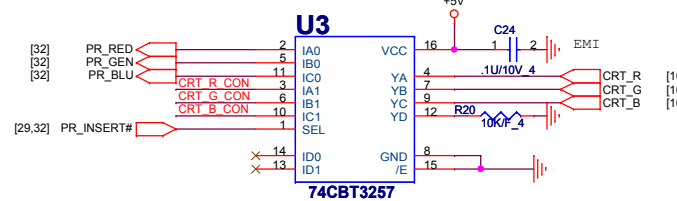
PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number LCD CONN/LID function	Rev 1A
Date: Monday, October 26, 2009		Sheet 21 of 45

CRT PORT

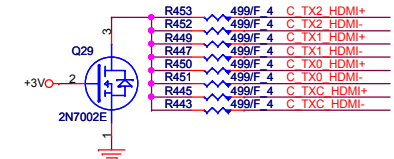
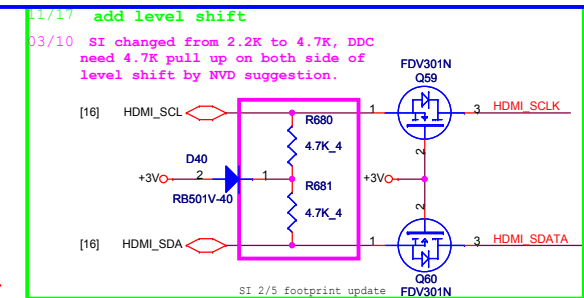
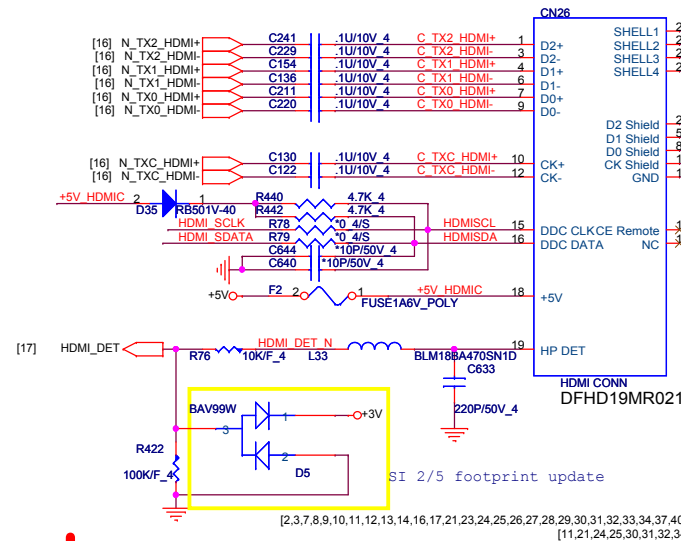


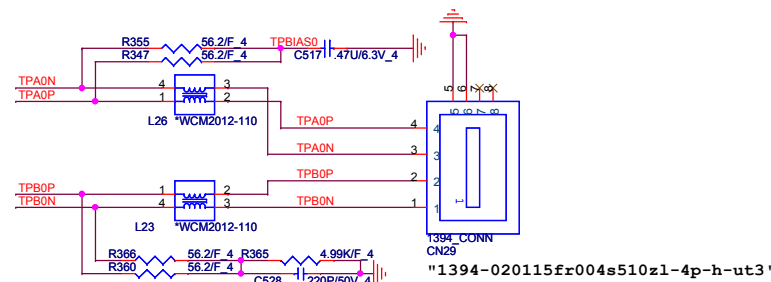
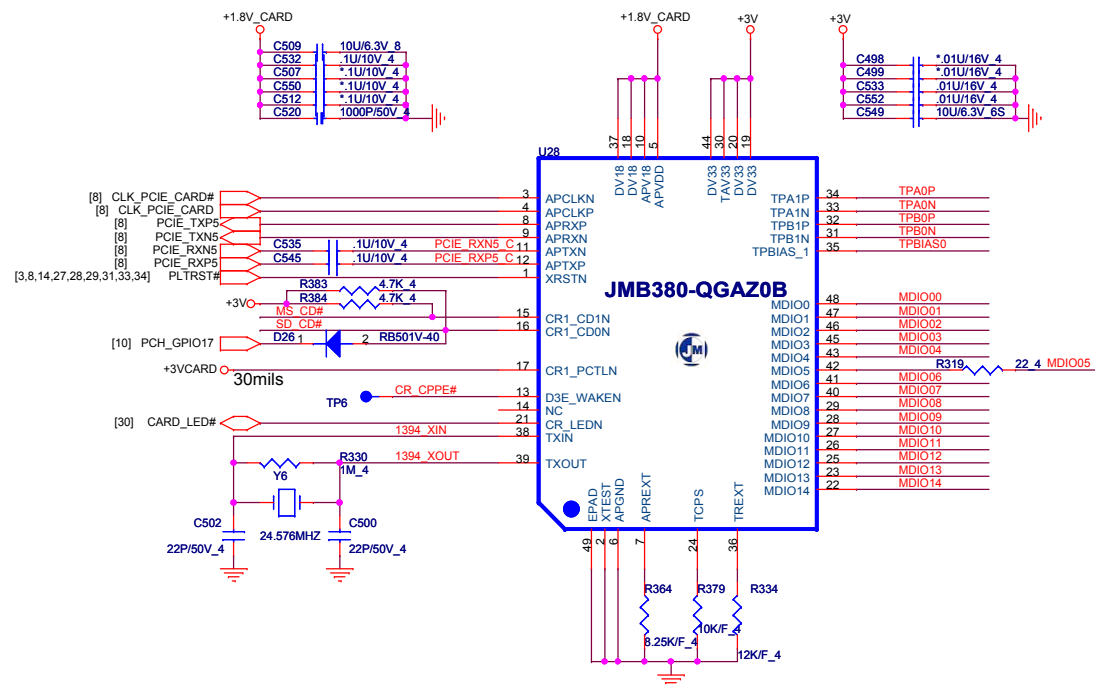
CRT SWITCH



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI PORT

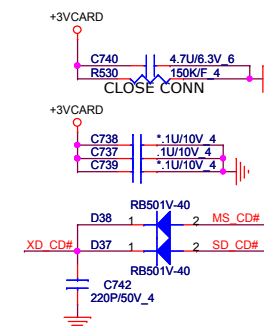
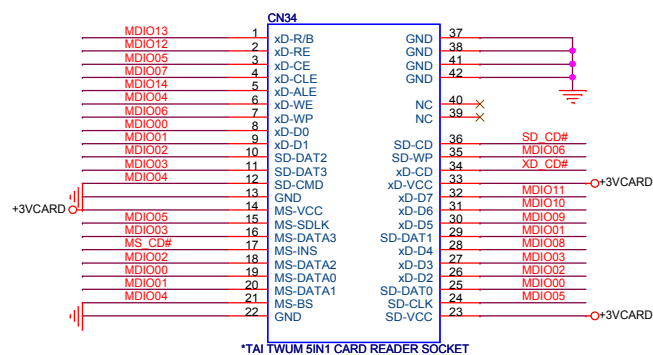
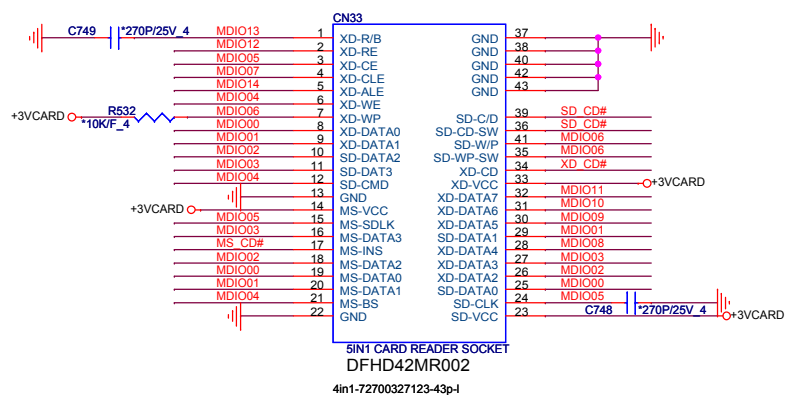




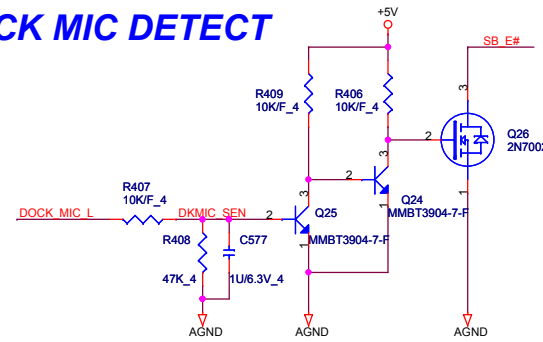
JMB 380 Note:

	SD/MMC	MS	XD
MIDI0	SD DAT0	MS D0	XD D0
MIDI1	SD DAT1	MS D1	XD D1
MIDI2	SD DAT2	MS D2	XD D2
MIDI3	SD DAT3	MS D3	XD D3
MIDI4	SD CMD	MS BS	XD WE#
MIDI5	SD CLK	MS SCLK	XD CE#
MIDI6	SD WP		XD WP#
			XD CE
MIDI7	SD DAT4		XD D4
MIDI8	SD DAT5		XD D5
MIDI9	SD DAT6		XD D6
MIDI10	SD DAT7		XD D7
MIDI11	SD DAT7		XD D7
MIDI12			XD RE#
MIDI13			XD R/B#
			XD ALE
CR1 LEON	SD1 LED#	MS1 LED#	XD LED#
CR1 CTLM	SD1 PCTL#	MS1 PCTL#	XD PCTL#
CR1 D0	SD1 CD#		XD C/#
CR1 CD0		MS1 CD#	XD CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP

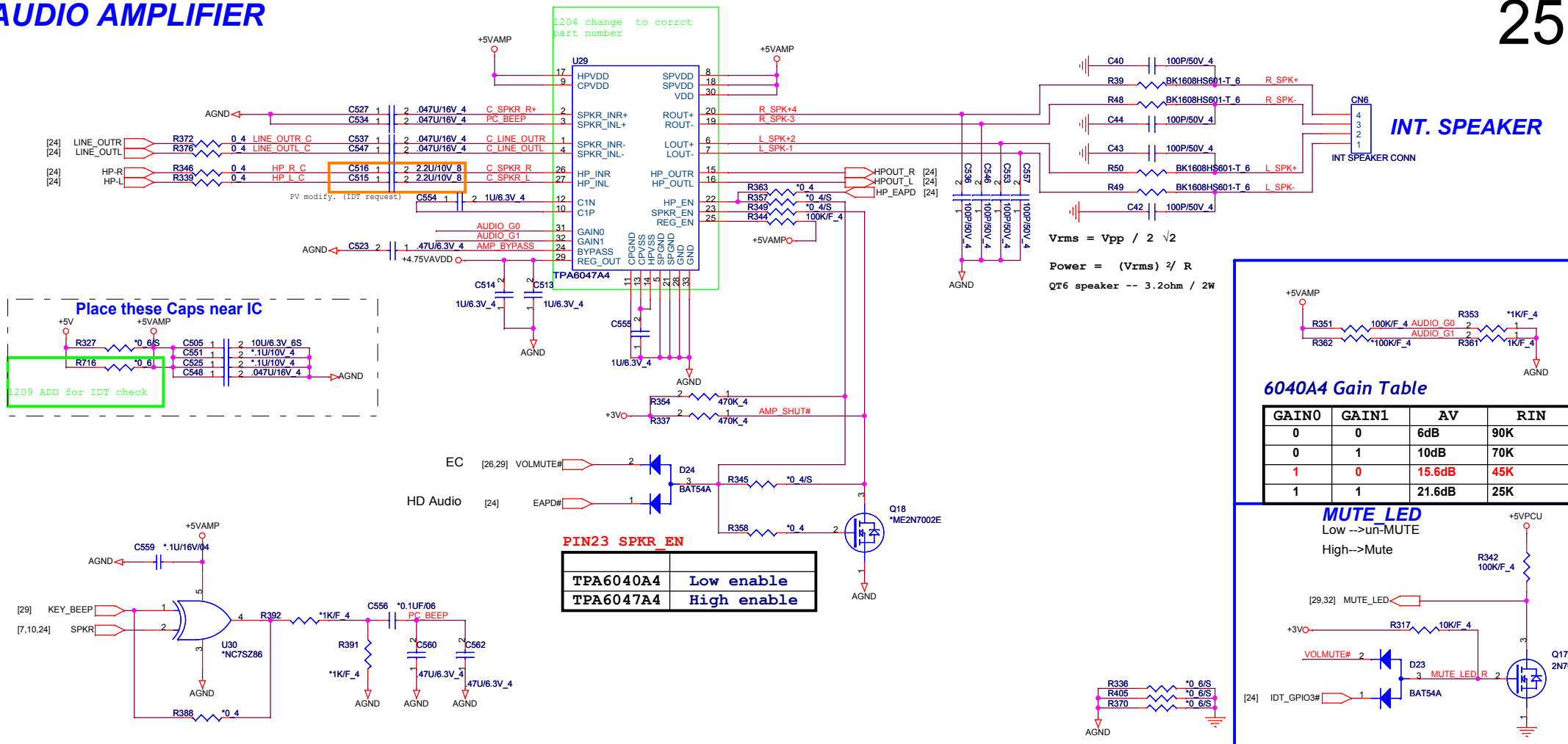


DOCK MIC DETECT



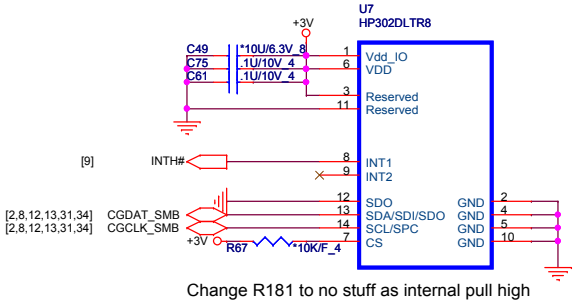
AUDIO AMPLIFIER

25



Accelerometer Sensor

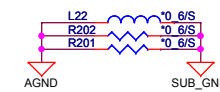
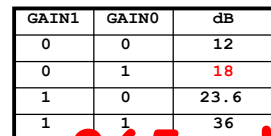
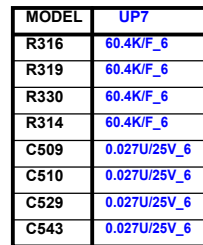
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

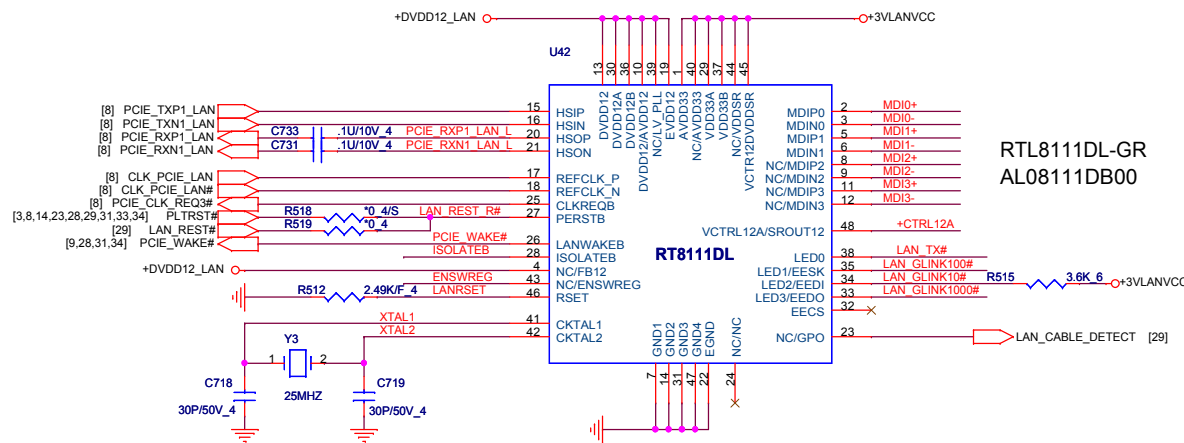


<http://sualaptop365.edu.vn>

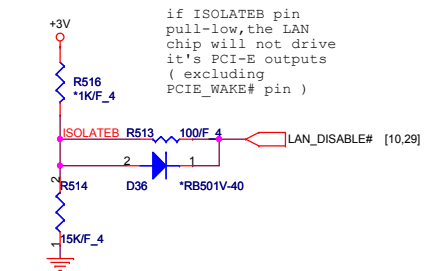
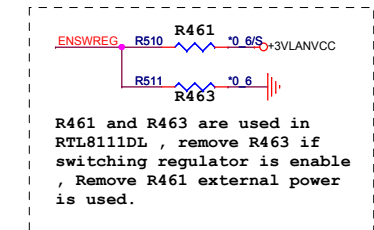
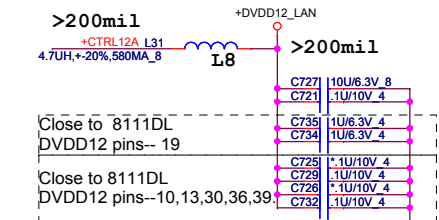
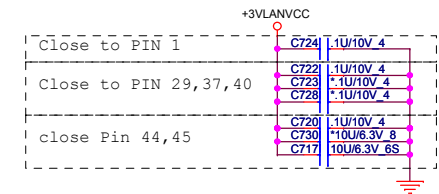
PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
AMP_TPA6047/Accelerometer		
Date: Monday, October 26, 2009	Sheet 25 of 45	

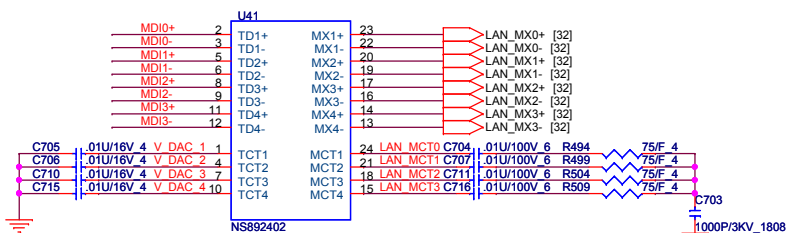




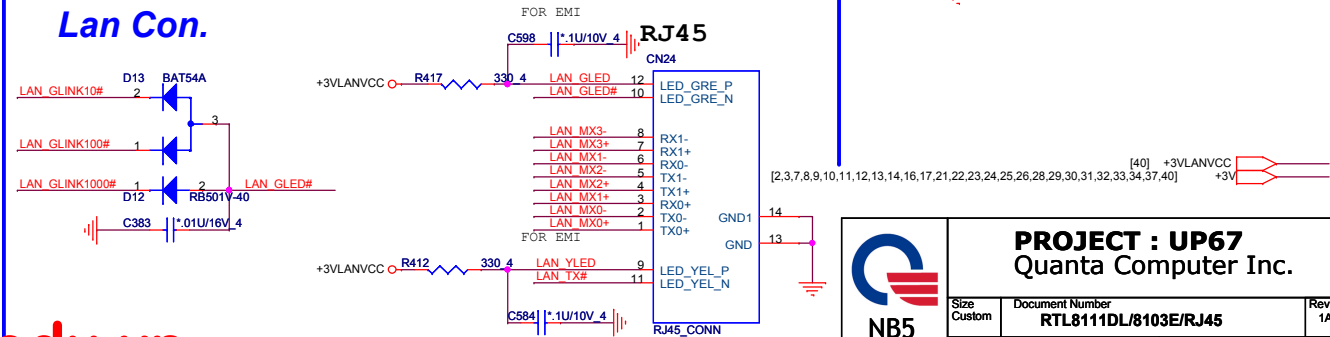
RTL8111DL-GR
AL08111DB00



Transformer for 10/100/1000



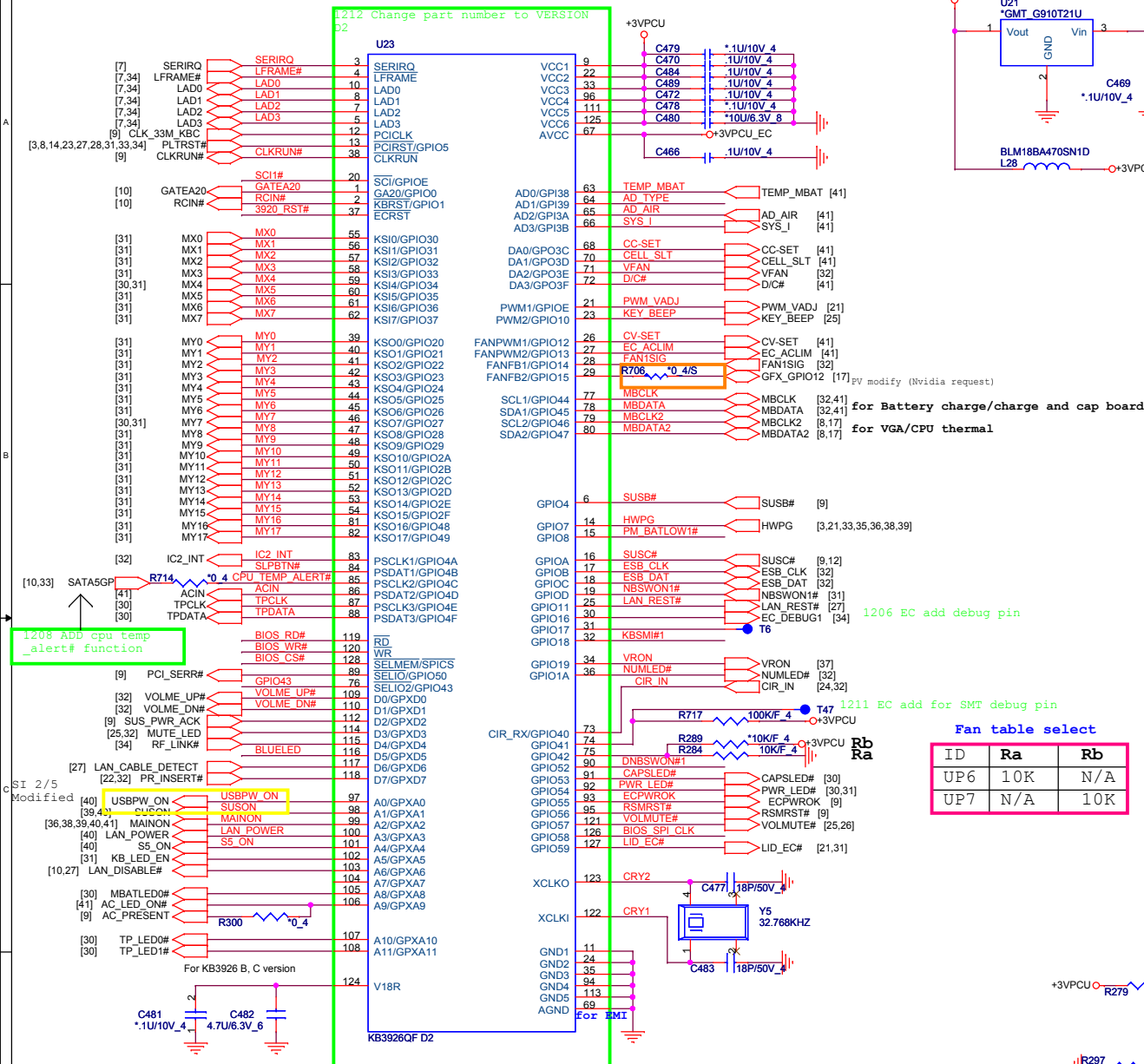
Lan Con.



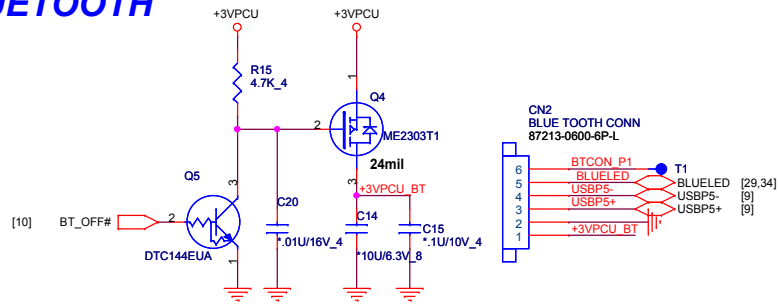
PROJECT : UP67
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL/8103E/RJ45	1A
Date: Monday, October 26, 2009	Sheet 27 of 45	

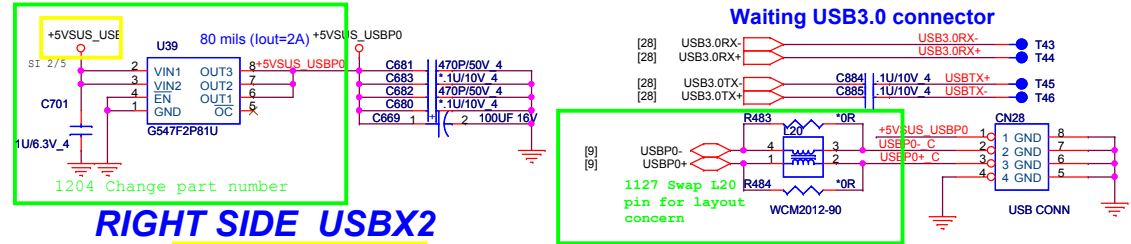




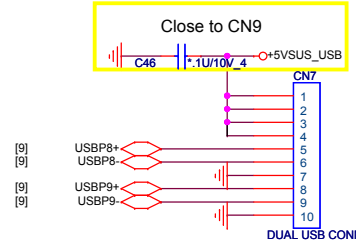
BLUETOOTH



LEFT SIDE USBX1 and E-SATA/USB COMBO

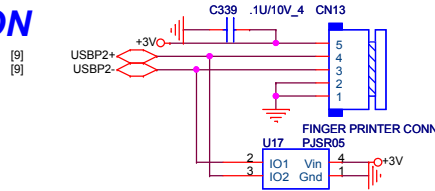


RIGHT SIDE USBX2



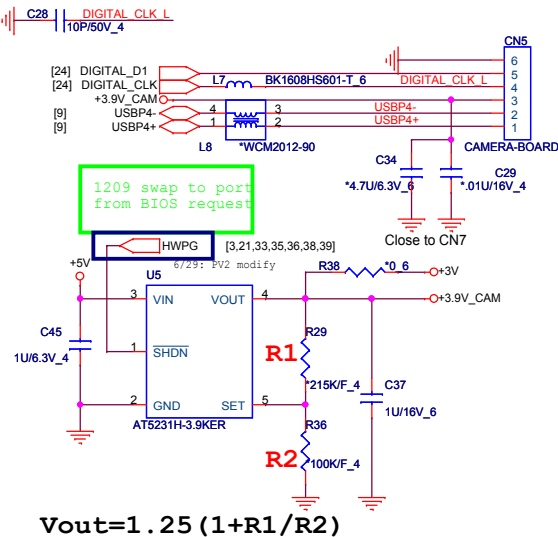
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

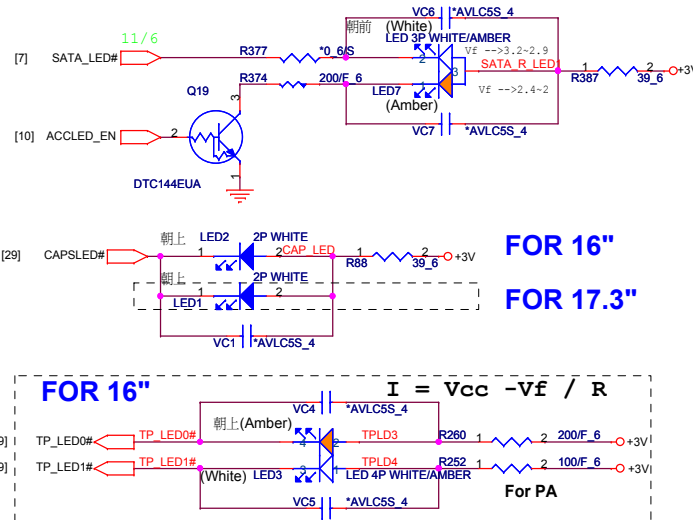


USB CAMERA /DIGITAL MIC CONNECT

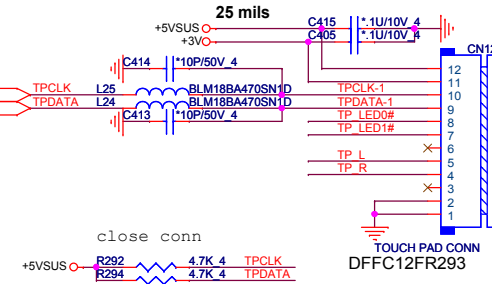
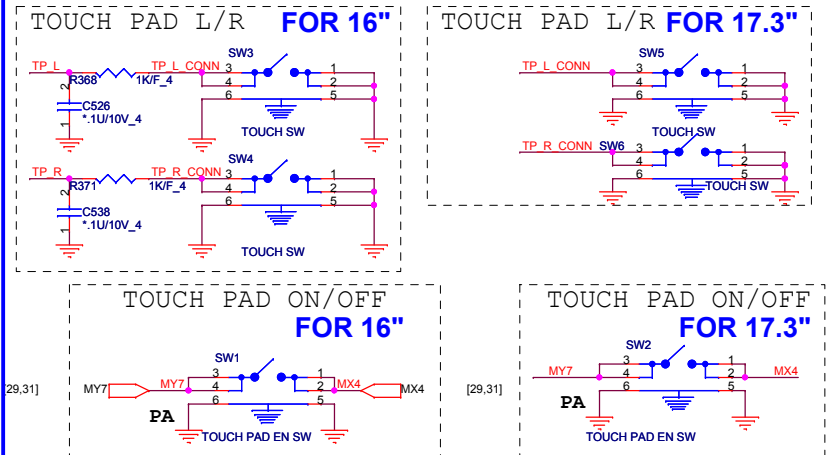
Add for EMI solution



LED



TOUCH PAD CONNECTOR & ON/OFF BOTTOM

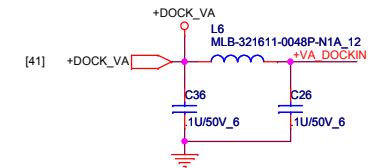


PROJECT : UP67
Quanta Computer Inc.

Size Custom Document Number BT/WC/FT/ESATA/USB/LED Rev 1A

Date: Monday, October 26, 2009 1 Sheet 30 of 45

32



[24]

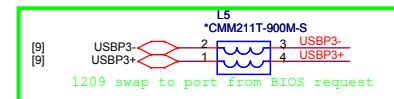
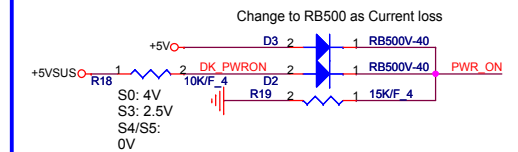
SPDIF

R404 221/F_4 C575 1U/50V_6

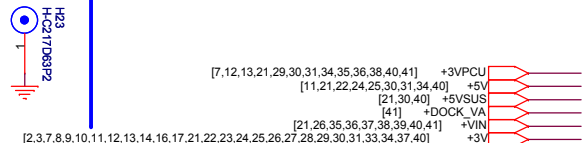
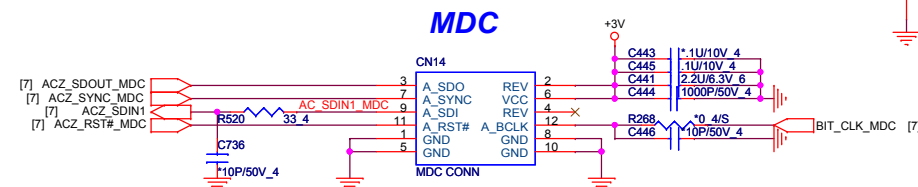
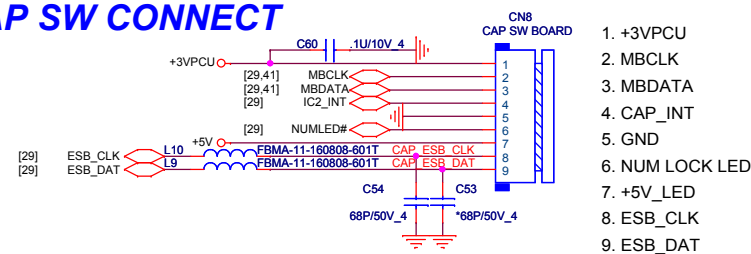
SPDIF_DOCK

R21 100/F_4 C25 220P/50V_4

[24] PR_INSERT#_IDT PR_INSERT#_IDT R352 PR_INSERT#

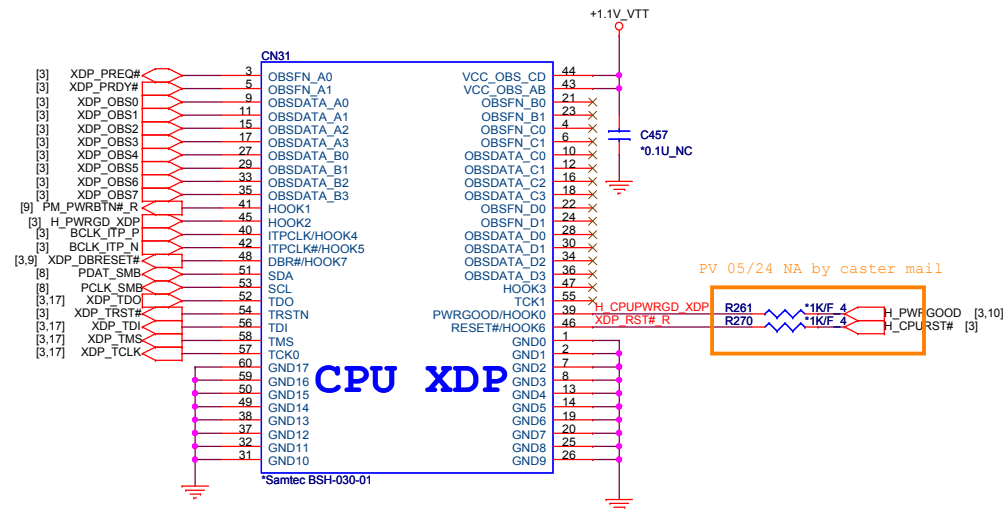


CAP SW CONNECT

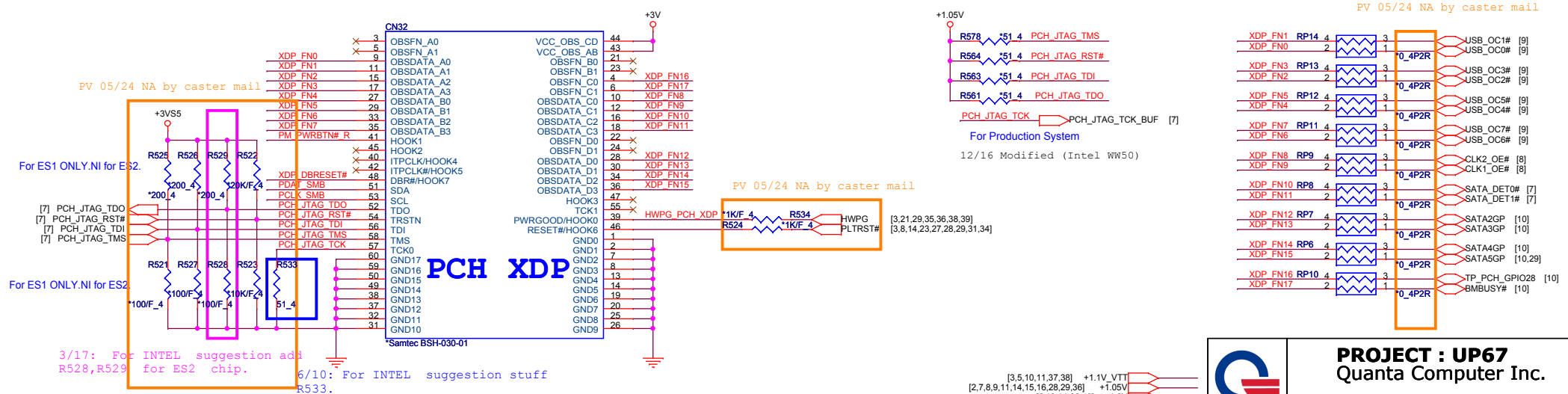
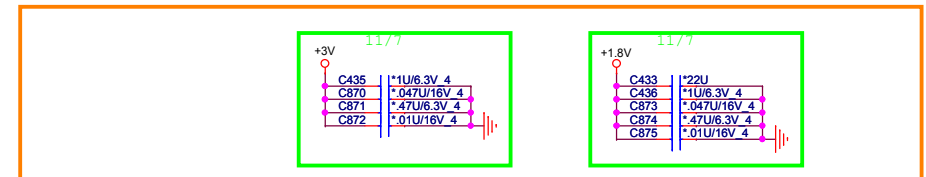
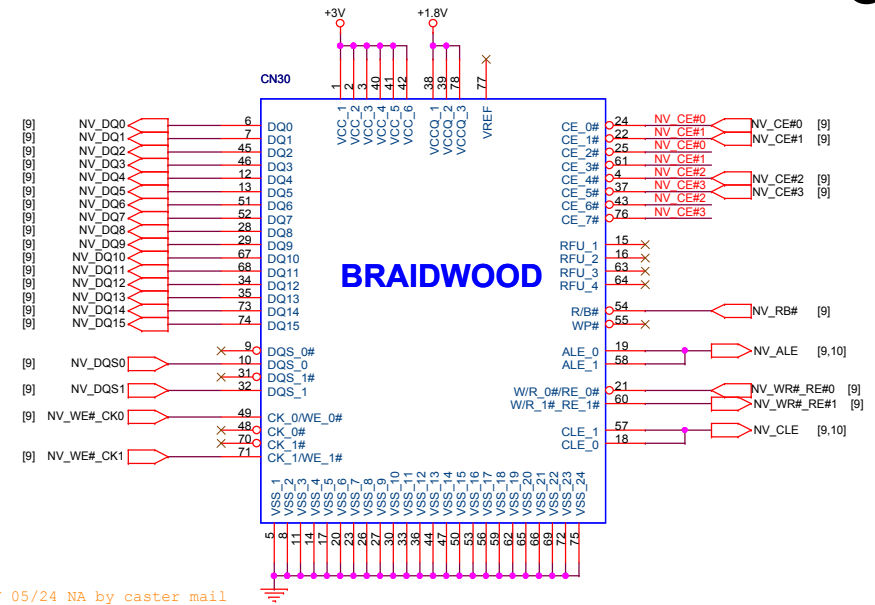
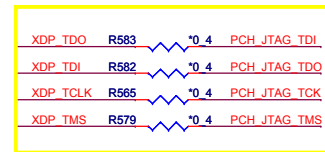


PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number DOCKING/FAN/CAP/MDC	Rev 1A
Date: Monday, October 26, 2009		Sheet 32 of 45

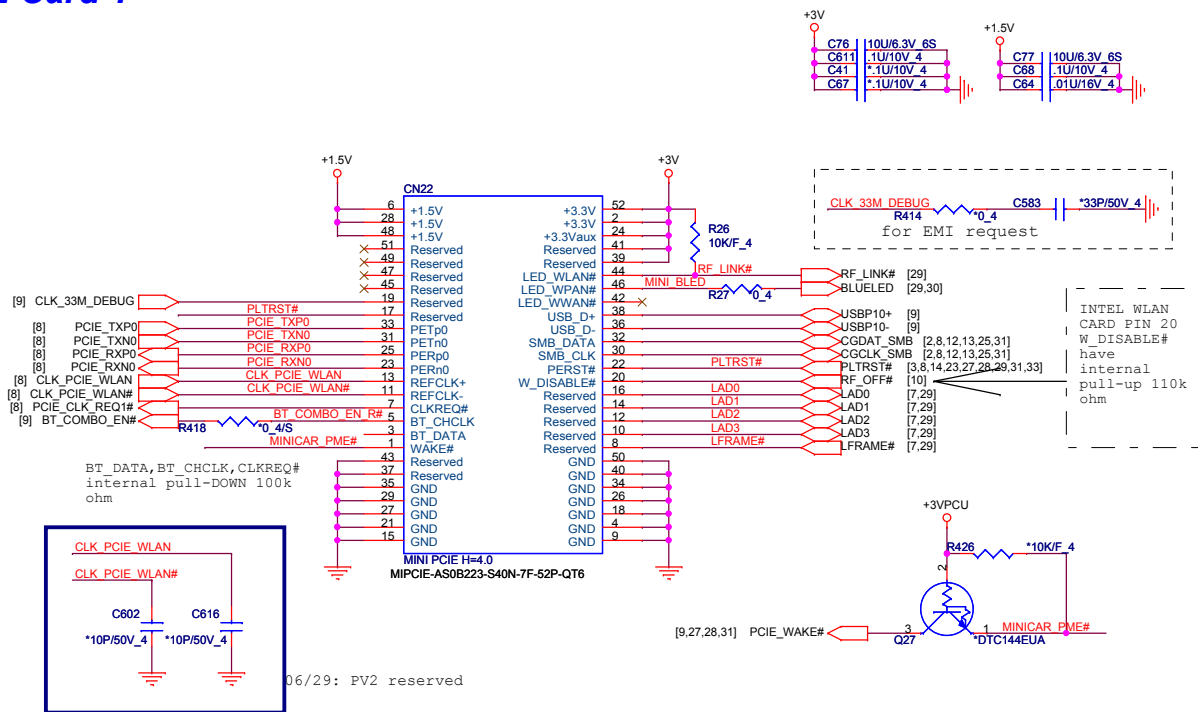


Reserve for BSDL

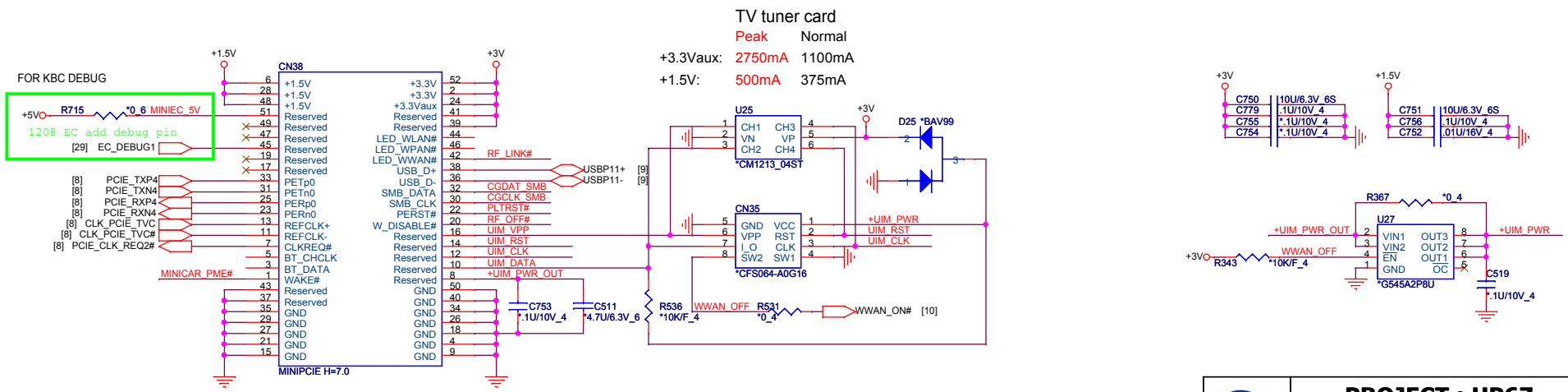


Mini PCI-E Card 1 WLAN

34



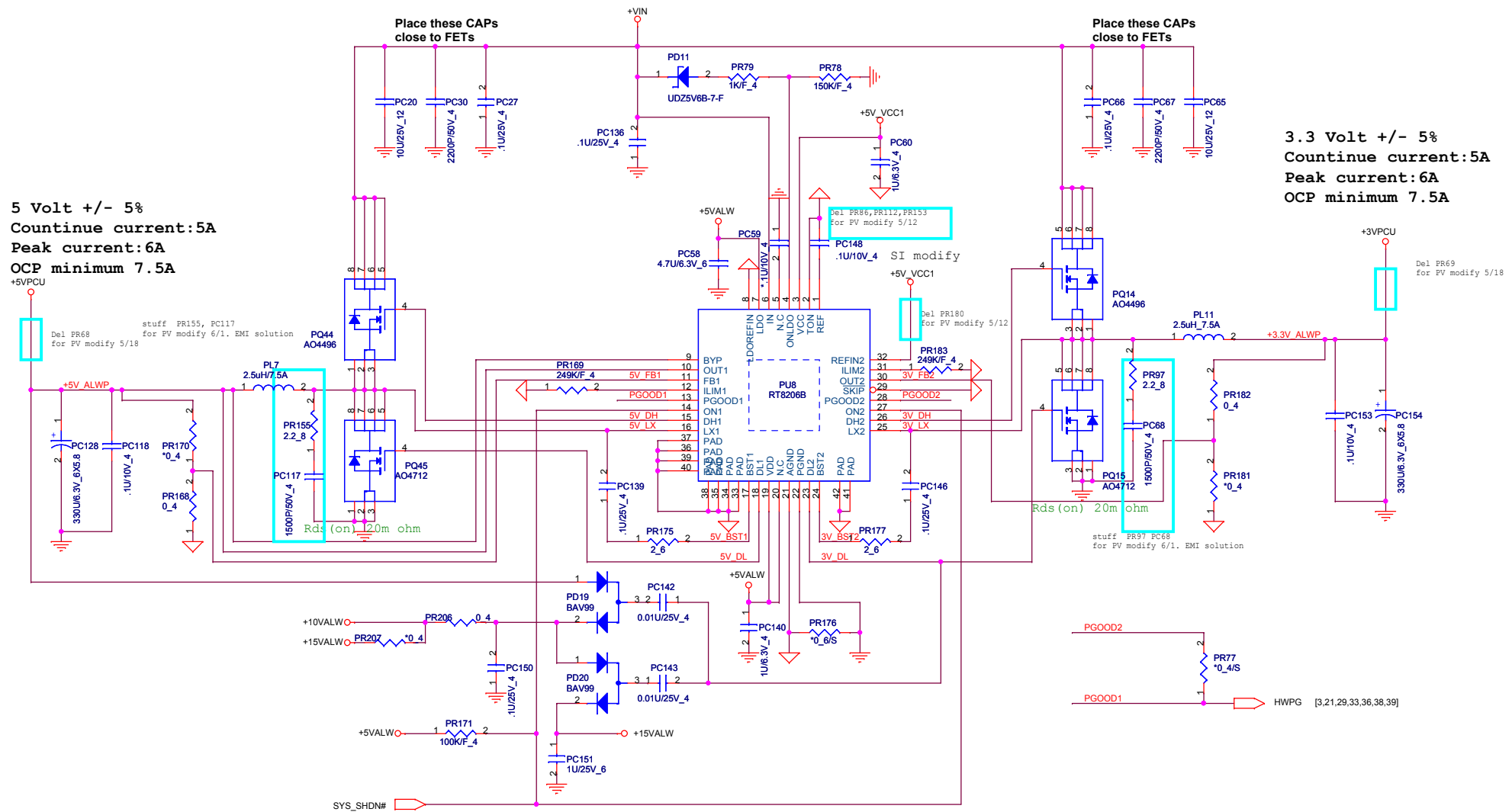
Mini PCI-E Card 2 TV Tuner or WWAN

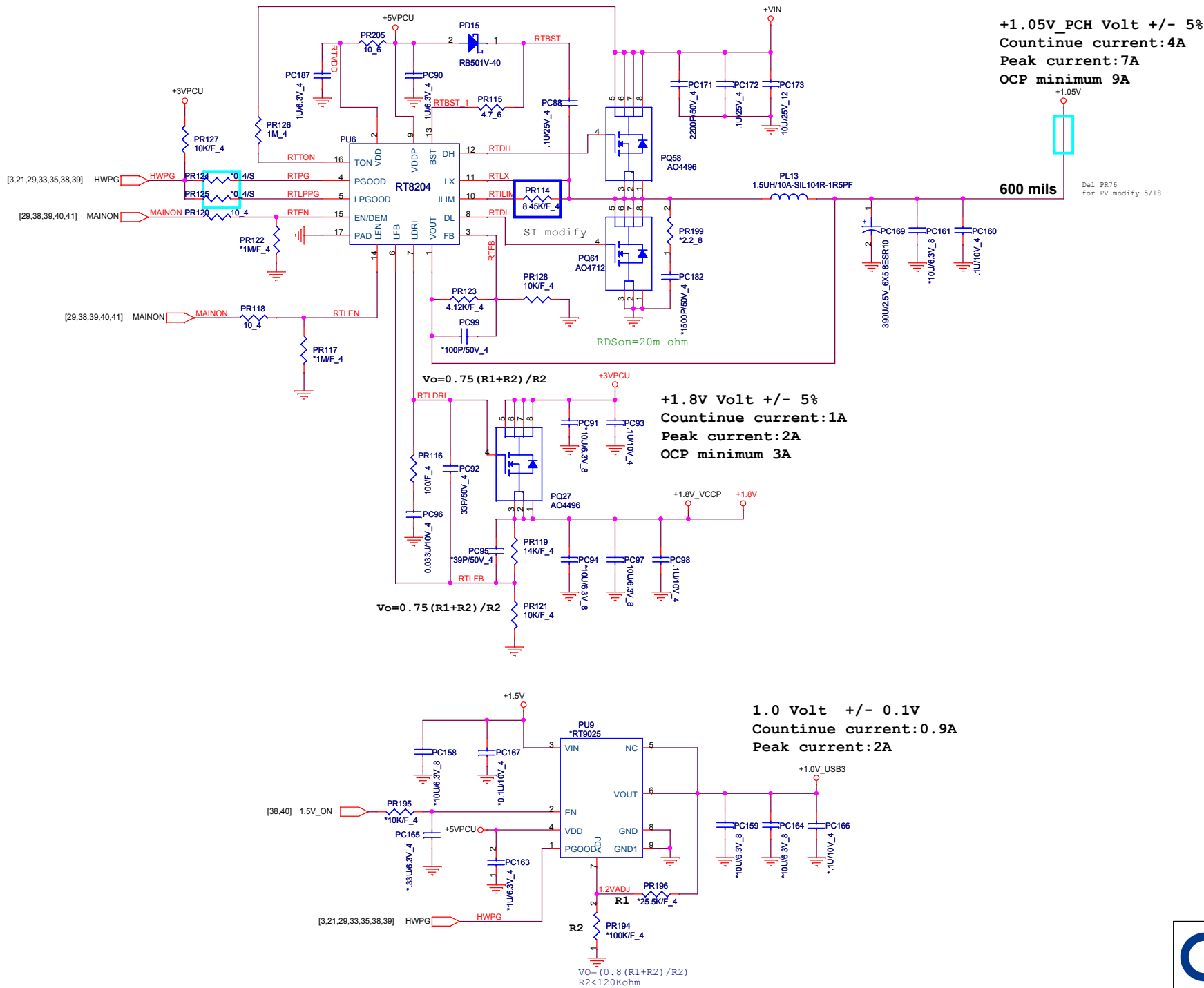


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PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN X2	Rev 1A
Date: Monday, October 26, 2009 Sheet 34 of 45		





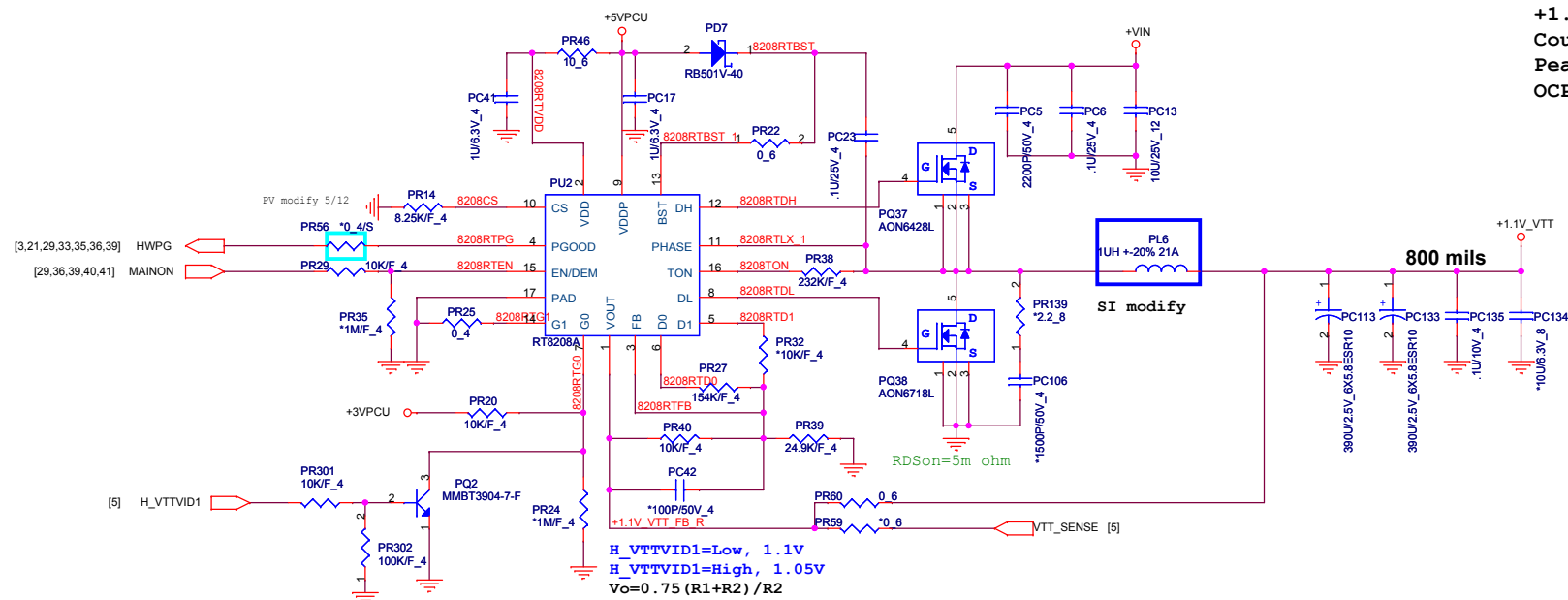
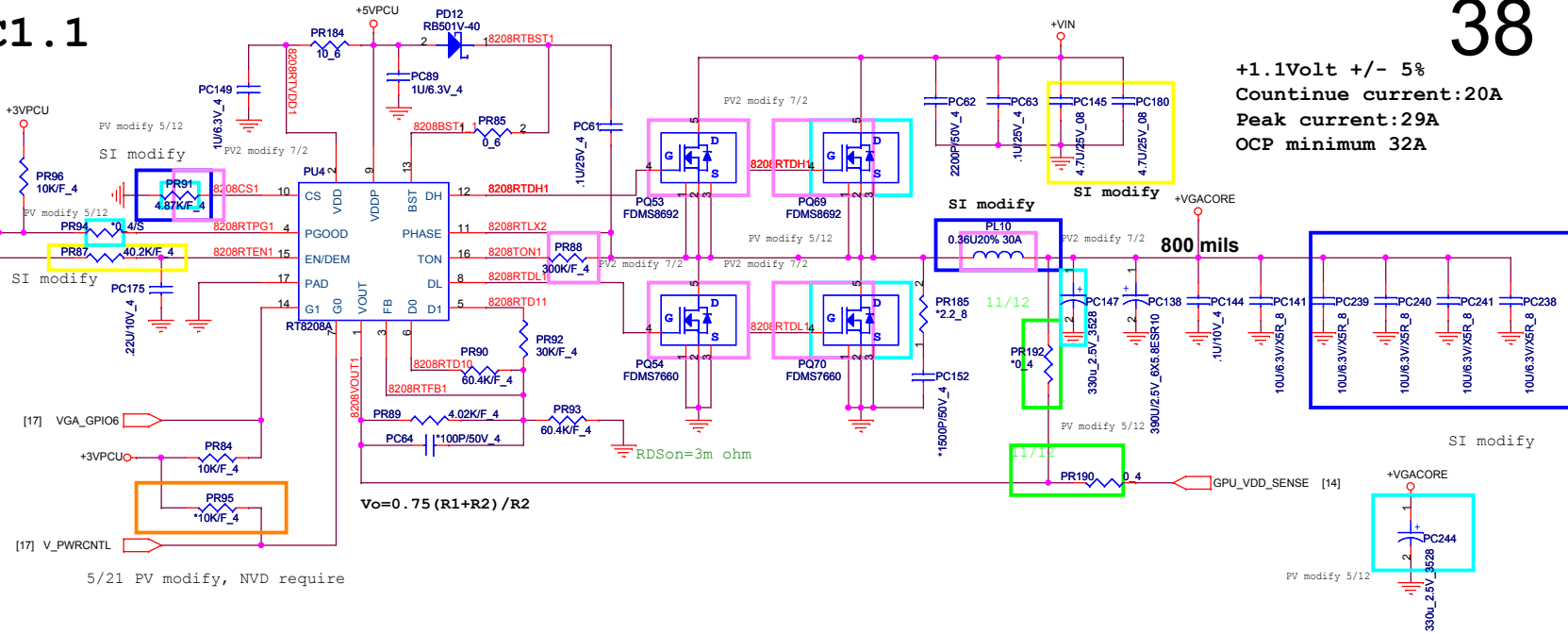
PROJECT : UP67
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A
Date: Monday, October 26, 2009	Sheet 36 of 45	



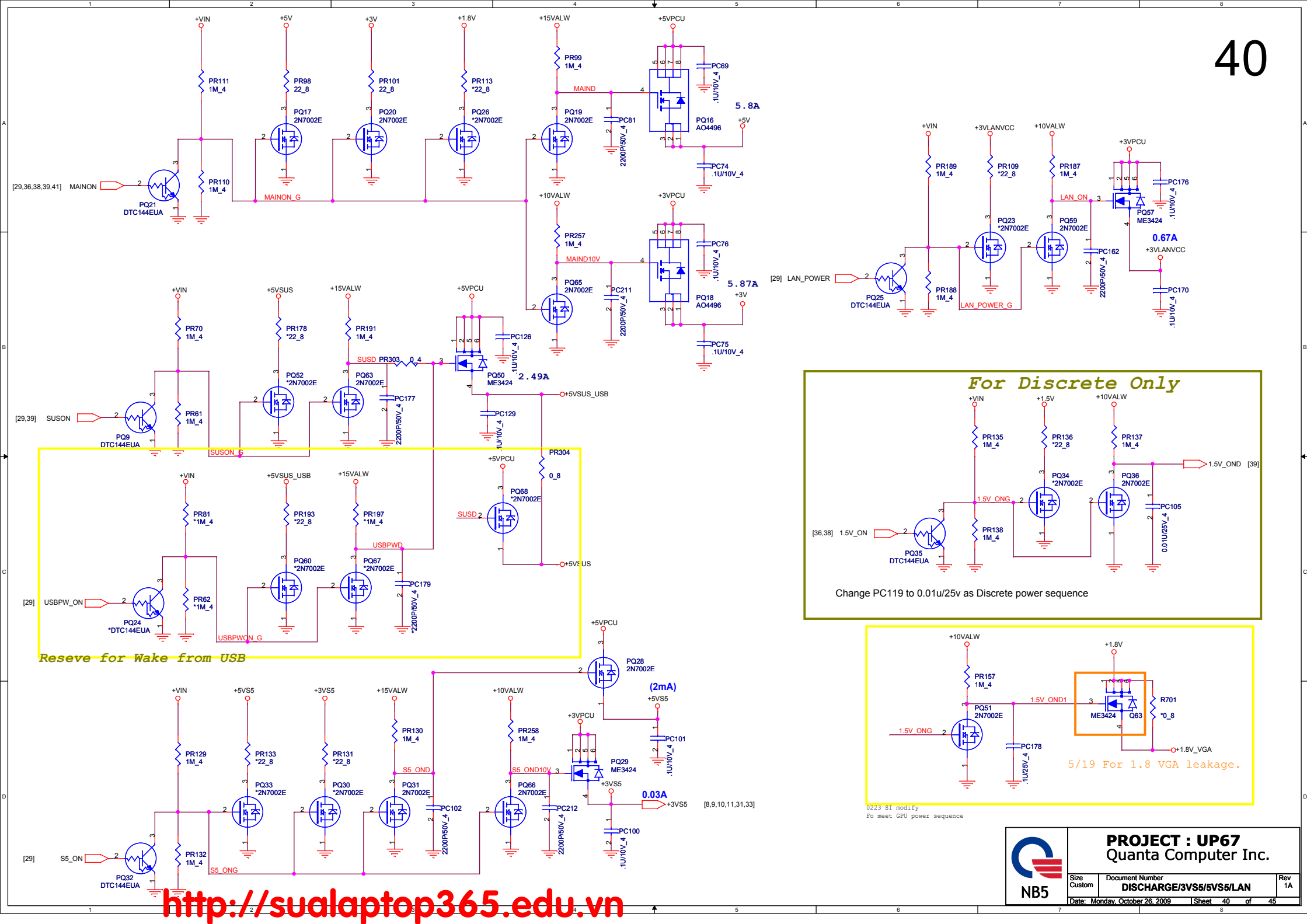
VGA Core & VCC1.1

VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V



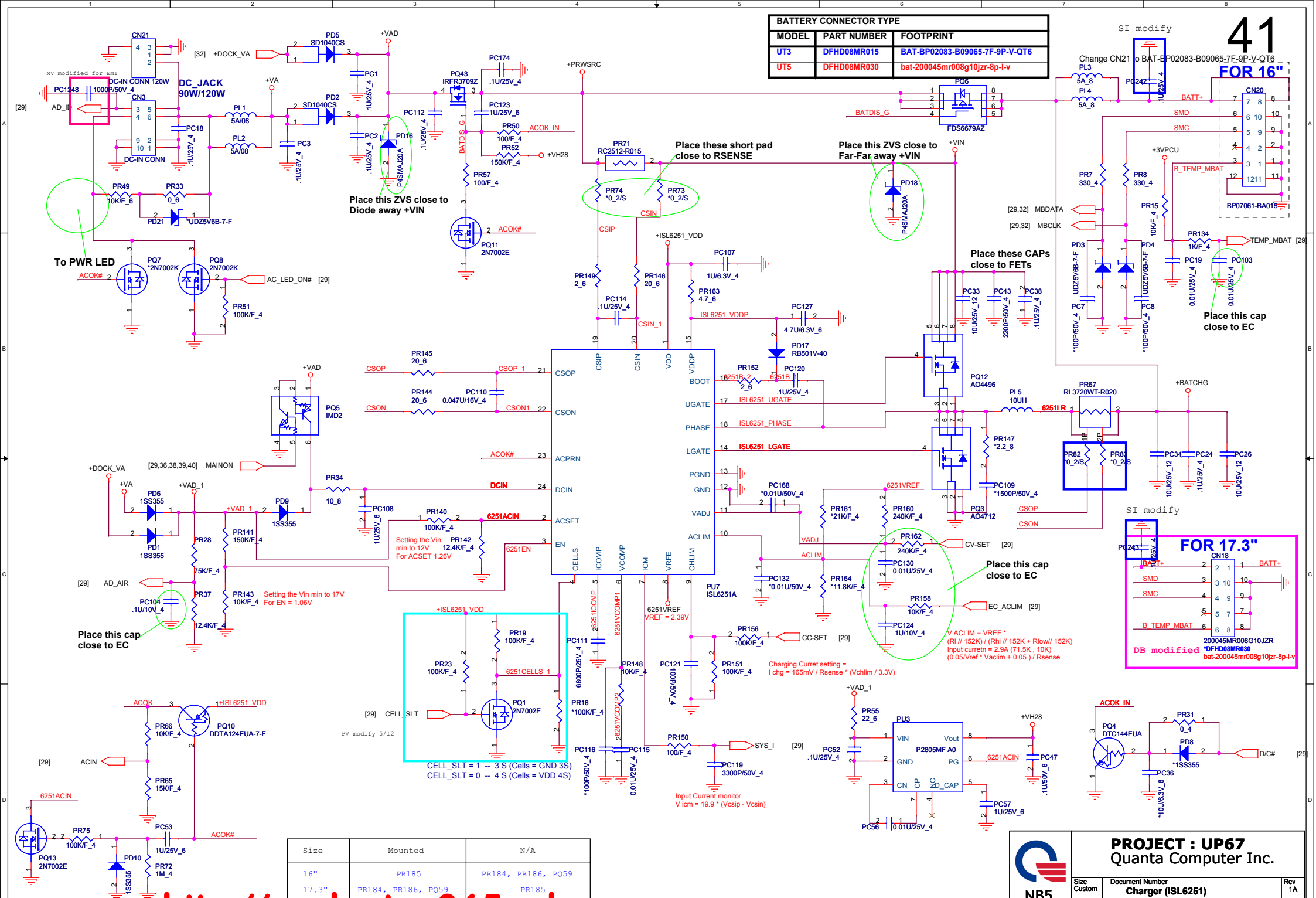
+1.1V_PCH Volt +/- 5%
 Countinue current:12A
 Peak current:15A
 OCP minimum 18A






BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

41
FOR 16"



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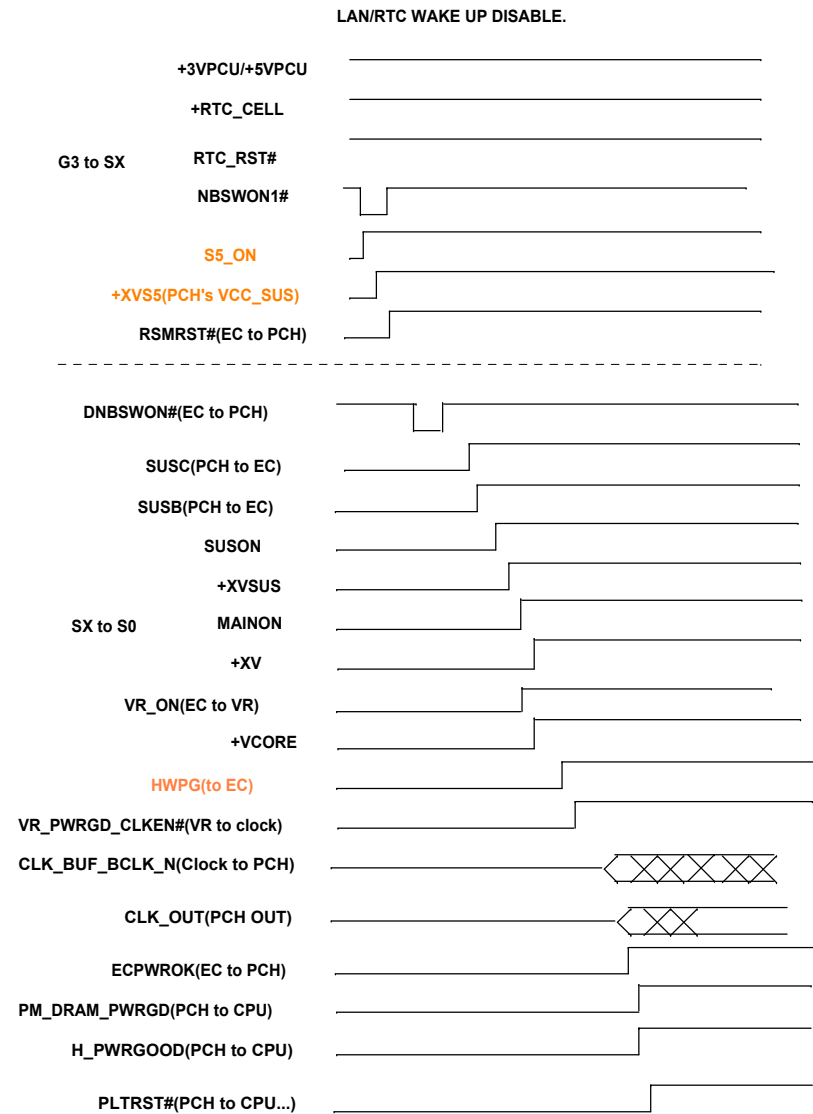
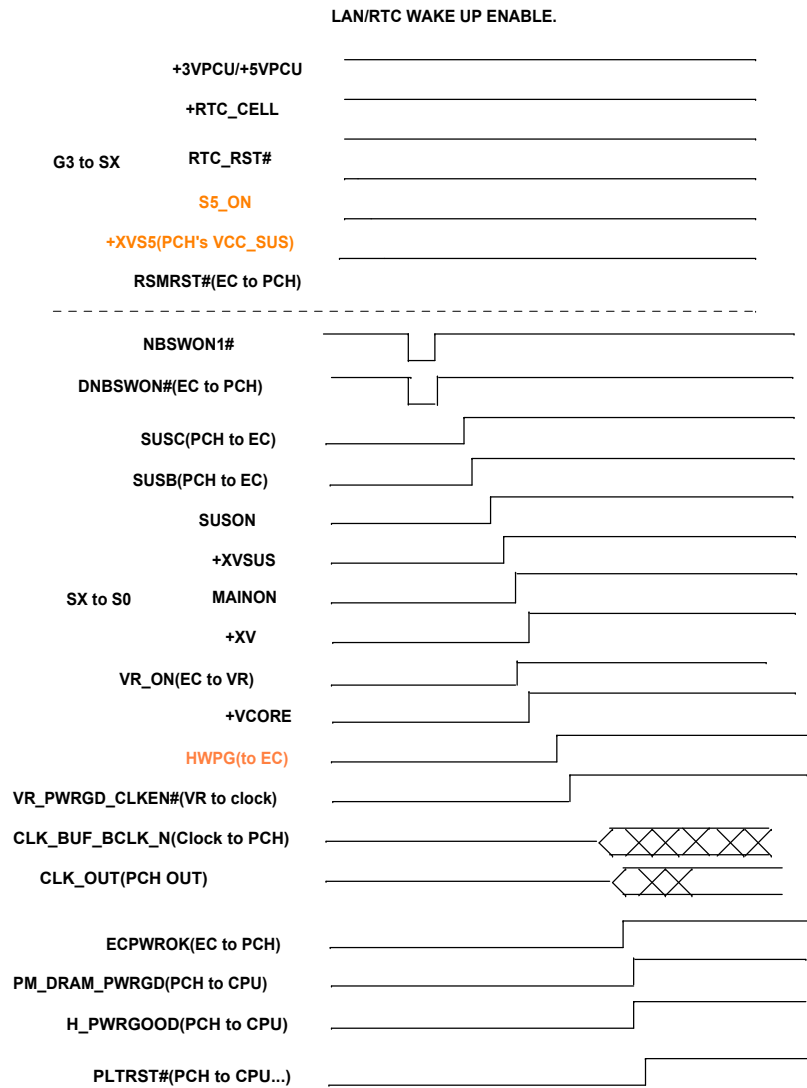


PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	Charger (ISL6251)	

Date: Monday, October 26, 2009 | Sheet 41 of 45

Power up sequence



PROJECT : UP67
Quanta Computer Inc.

Size Custom	Document Number Power up sequence	Rev 1A
Date: Monday, October 26, 2009 Sheet 42 of 45		